

Circuit design for high temperature hybrid manufacturability

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Abstract

High-temperature hybrids have been demonstrated to be the most reliable packaging method for down-hole circuits which will be subjected to elevated temperatures, thermal cycling and/or high shock and vibration. However, one cannot simply take a standard surface mount circuit and repackage it in hybrid form and expect good results. The circuit designer must consider issues such as die availability and active component functionality at high temperature. Passive components may also need to be changed: considerations include the availability of resistors and capacitors of appropriate physical size in hybrid-compatible packages, component tolerances over the temperature range and the effects of aging on these components. Practical hybrid package size limitations are driven by ceramic processing capabilities, dimensional tolerances, and thermal expansion mismatch between the substrate, the components, and the outer package. Circuit size reductions are not always realized as allowances must be made for package wall thicknesses, I/O pins, clearance between components and clearance for automated wire bond tools. Ten years of continuous hybrid process development and extensive circuit reliability testing has exposed several limitations on assembly reliability. Lessons learned and statistical failure data will be presented..

Limitations of SMT technology

Most down-hole electronics circuits used today are made using surface-mount technology (SMT). Circuit boards are typically made of polyimide, and are assembled with various solders, including SnPb, SnAgCu and SnAg. The useable life of these boards is limited in the high temperature and high vibration environments common in deep oil and gas wells. Quartzdyne has conducted continuous testing since 1994 [1], [2], [3] to monitor the quality and expected lifetimes of various circuit technologies, including SMT. This testing has exposed several limitations of SMT in high temperature environments.

A major cause of failure in SMT assemblies is degradation of wire bonds within plastic encapsulated microcircuits (PEMS). Au wires are routinely bonded to Al IC pads in almost all commercial PEMS. This interface is prone to Kirkendall voiding [5]. Failure times of about 3000 hours at 180°C can be expected due to degradation of the Au-Al interface [6]. The degradation is accelerated by Bromine fire-retardants commonly used by many vendors, which reduce the life time to as little as 750 hours in the same test [4], [7]. Increased solder temperatures of Pb-free and high melting point solders further exacerbates this problem, where a significant portion of the life of the product is used up in the 260°C to 320°C soldering process.

Solder failure can also be an issue with SMT boards. TCE mismatch between the components and the board can cause solder fatigue, particularly with the more brittle Pb-free solders such as SnAgCu and AuSn commonly used in down-hole assemblies. As these assemblies are subjected to thermal cycling, cracks in non-compliant components or the solder joint are possible (Figure 1-a, b).

Another limitation of traditional surface mount assemblies is the polyimide board itself. In our experience, board life is limited to approximately 750 hours at 225°C, at which point most of the polyimide material has decomposed leaving behind a fragile web of fibreglass and metal traces (Figure 1-c). This is an issue for both SMT and through-hole designs.

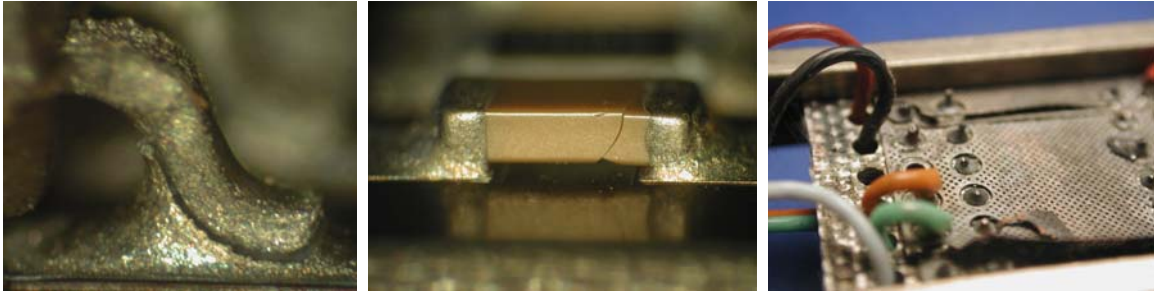


Figure 1. Common failure modes in traditional SMT assemblies (left to right): (a) open solder joint, (b) cracked capacitor, (c) polyimide degradation.

Introduction to Hybrid technology

Hybrid technology consists of multiple bare die, along with passive components mounted to a ceramic substrate in a single ceramic and/or metal package. These assemblies are also referred to as multi-chip modules (MCM). While more costly than SMT technology, the hybrid approach provides several advantages in harsh environments.

By eliminating the plastic package encapsulating the die and using Al instead of Au for the wire bonds, orders of magnitude more reliability can be achieved. Ceramic substrates offer better high-temperature performance than do polyimide-based materials. Better thermal matching between the ceramic substrate and the components provides for lower-stress mounting and thus better thermal-cycling properties. Hermetic packaging further protects the mechanical and electrical interfaces within the hybrid from degradation with exposure to high temperatures for extended periods of time. In our testing we have been able to achieve typical survival times of 3000 hours at 250°C using carefully chosen hybrid assembly processes. In comparison, SMT assemblies show routine failure at 3000 hours at 150°C (Figure 2).

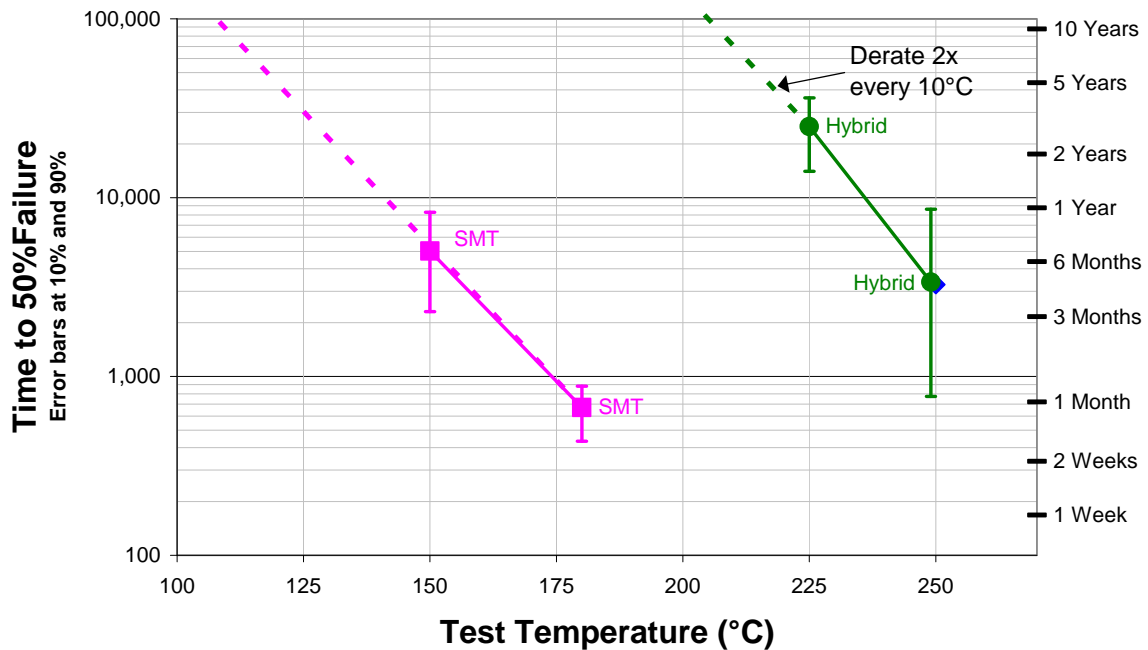


Figure 2. Survival time of circuits in un-powered aging and thermal cycling tests performed at Quartzdyne from 2003-2007.

Hybrid Manufacturability Considerations

So why don't more people use hybrids down hole? Parts availability and cost have been the major barriers. High temperature hybrids are rarely cost-competitive with surface mount. The lower-cost hybrid technologies offered for commercial applications are usually not appropriate for down-hole, as many of the commonly used materials and processes do not yield good high-temperature performance. Materials must be chosen which can survive the harsh down-hole environment. While these materials are well known, few hybrid vendors use them because of increased costs and processing complexity. Tooling for substrate manufacturing can be 5-10 times more than for an equivalent SMT board. Component costs are also significantly higher than their SMT compatible counter-parts, and hybrid-compatible component selection is limited.

The high temperature market is sufficiently small that few part vendors are willing to cater to it. Mainstream commercial parts tend to sell in quantities of millions, while high temperature down-hole quantities are more often in the hundreds to thousands range. The extra cost of designing and qualifying parts for high temperature is difficult for commercial vendors to justify, and so most vendors simply choose not to.

With high costs, limited parts availability, and few vendors supporting the high temperature parts and processes, it is not surprising that relatively few companies offer hybrid products for down-hole tools today. As the reliability of the present alternatives decreases, and the demand for higher temperature down-hole tools increases, the tables will turn and most companies servicing the down-hole industry will need to incorporate hybrids into their product lines to remain competitive. The transformation from SMT to hybrid is not trivial: designs will need to be modified to deal with the limitations of the hybrid process. In the following sections we will discuss some of the issues most likely to confront the first-time hybrid circuit designer.

What kind of Package?

When choosing a hybrid package, the designer must consider the space requirements for components and traces, the space for I/O interconnects, how the entire package will be mounted, and how external components will be connected. The two most common packaging options for high-temperature hybrids are thick-film ceramic substrates mounted in Kovar packages, and high-temperature co-fired ceramic (HTCC) packages (Figure 3). The trade-offs between these are discussed below.

In the first option, a Kovar package is either machined or stamped. This package can incorporate a variety of mounting options including mounting tabs and blind-threaded holes. Pins are mounted in the package with glass insulators and can exit either the sides or bottom of the package. The pin-count is limited by the length of the sides, so this package type is primarily used for low pin-count systems. The glass seal around the pin is somewhat fragile, so care must be taken when soldering to the pins not to fracture the glass, potentially compromising the package's hermetic seal. The package lid is sealed with a parallel seam-sealer in a clean nitrogen environment. A thick film or HTCC ceramic substrate unique to each design is bonded into the package. Since the substrate is manufactured separately from the package, design modifications on the substrate do not necessarily require changes to the package. In many situations a stock package can be used. Size limitations are primarily associated with the ceramic substrate processing. Most fabrication houses will not process boards greater than three inches in length, and aspect ratios greater than 4:1 are not recommended.

HTCC packages are built up with a series of "green" flexible ceramic layers. Each layer is punched, stacked and printed with metal trace layers before the entire stack is fired. After firing, Kovar rings and pins can be brazed to the package allowing for complex package geometries. This is the process used to create most standard ceramic packages including pin-grid arrays (PGA) and ceramic quad flat packs (CQFP). Pin-counts can be relatively high, so this package is preferred for modularized designs with a large number of interconnects. A braze ring allows welding a Kovar lid similar to the Kovar package described above. The more traditional option is to attach a Kovar lid to the ceramic package using AuSn solder. Either process can be performed reliably, however the welding process is considered to be cleaner and thus preferred in Hi-rel applications. Since the ceramic shrinks as it cures, dimensional tolerance is a significant factor with HTCC substrates, particularly with large designs. Tooling costs can be significant for complex package geometries.

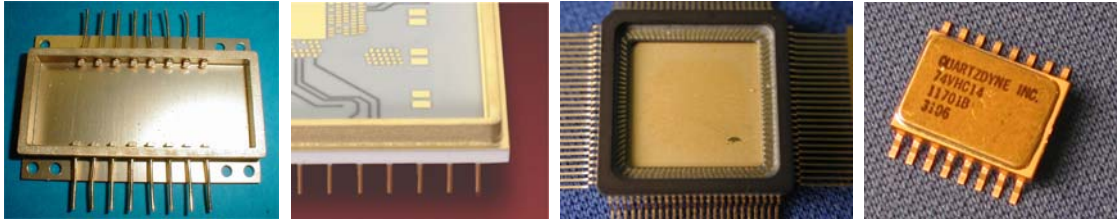


Figure 3. Sample package types: (left to right) Kovar package with glassed pins, HTCC with braze ring, HTCC Quad Flat-Pack, ceramic SOIC with soldered lid

Board Space Requirements

Hybrids offer some degree of miniaturization. Ironically, line width and spacing requirements for hybrid substrates are actually greater than those of surface mount assemblies. This is because traces are screen-printed, not etched. An 8 to 10 mil line and space requirement is typical for ceramics, where 4 mil spacing is achievable in typical SMT designs. Via top layer requirements can be as high as 15 mils for cover pads (Figure 4-b).

There are additional spacing requirements beyond the limitations of the printing process. Spacing requirements around a capacitor or large die pad, for instance, are as high as 30 mils because of the potential for conductive polyimide squeeze-out (Figure 4-a). Another consideration is capacitor-to-capacitor spacing where side-access is required to apply non-conductive staking materials (Figure 4-c). A commonly overlooked spacing requirement is bond-head clearance beyond a wire bond target during the tear-off phase of wedge bonding (Figure 4-d).

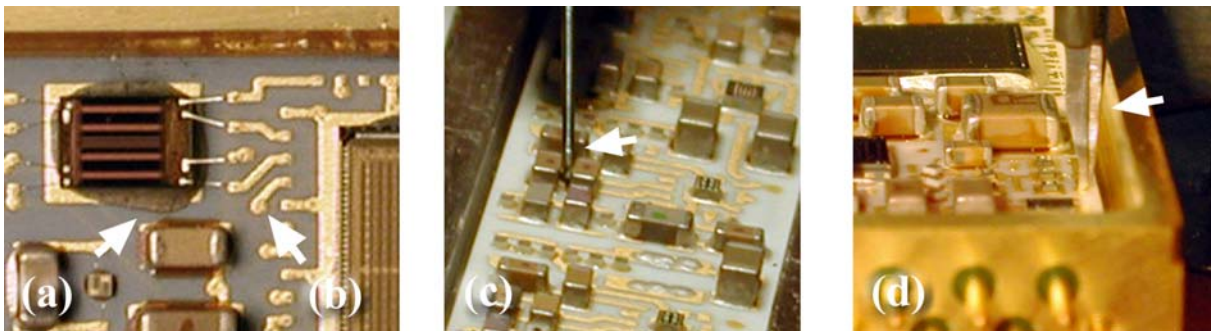


Figure 4. Spacing requirements: (a) Polyimide bleed-out on die and caps, (b) minimum trace and via spacing, (c) clearance for tools between capacitors and (d) clearance around wire bonding tip.

Die availability

It may seem counter-intuitive that bare die can be so difficult to acquire. The reality is that commercial vendors typically package millions of semiconductor devices using high-speed packaging equipment which takes untested die from a cut wafer, and then places, bonds, and encapsulates the devices with little human intervention, and at a very low cost per unit. Packaged devices are then tested in relatively inexpensive high-speed testers before being sorted and shipped to distributors. Testing at the wafer level is extremely difficult and time-consuming. Devices must be probed using precision automated equipment that contacts microscopic bond-pads on each device. The probing process itself can damage the pads or surface of the die. Tests at elevated temperatures create additional problems requiring wafer heaters and high-temperature probe cards. Subsequent handling and packaging of the tested die is also a tedious process that most semiconductor vendors are not set up to do. When bare die is acquired, it is often only available as full and untested wafers, with the subsequent steps of testing, cutting, and waffle-pack packaging being completed by a subcontractor. In this case the customer is usually forced to buy an entire wafer which may contain 10's of thousands of devices when only a few hundred are needed. The majority of commercial die vendors simply will not sell bare die, so the designer is limited to working with the few vendors who do – and on their terms.

Another consideration is the functionality of the die at high temperatures. There is a limited, but growing set of die available that are specifically designed for high temperature use [8], [9]. The offerings are far from complete, however so standard commercial parts must often be used. When choosing commercial parts, the individual functionality of each part must be considered. Simpler parts on larger processes tend to fare better at high temperature. We have pushed VHC glue-logic chips as high as 280°C. Other more complicated parts such as microcontrollers, FPGA's, Op-Amps

and voltage references can be found that work at temperatures greater than 200°C, but each must be qualified for the specific application.

Discrete Transistors vs. Monolithic Arrays and ASIC's

Different sized semiconductors must be mounted differently. In our experience we have found that small bulk discrete devices cannot be held with conductive polyimide – there is insufficient strength in the small area to create a reliable attachment [2]. We have found eutectic solder attach to be much more effective for small devices where a conductive attachment is required. With larger devices, the eutectic attach does not provide sufficient compliance during thermal cycling and therefore, polyimide or thermoplastic is preferred. The eutectic attach process is complex and time-consuming, requiring an individual heat, pressure, and scrub cycle for each component. Continued thermal cycling associated with processing multiple devices negatively affects the parts placed first. In our experience, process yield is significantly reduced when more than 10 devices are attached with this method. One alternative to discrete devices is to use monolithic transistor arrays. These are available in both bulk and SOI processes. Another alternative is to consolidate designs into custom application specific integrated circuits (ASIC). The entry-level costs for implementing ASIC design and fabrication have decreased dramatically over the last few years. Where standard devices are not available, an ASIC may be an affordable option even for relatively small product runs [10]. The two circuits of Figure 5 are functionally equivalent, but the top version which uses a transistor array and an ASIC has significantly better manufacturing yields and long-term reliability.

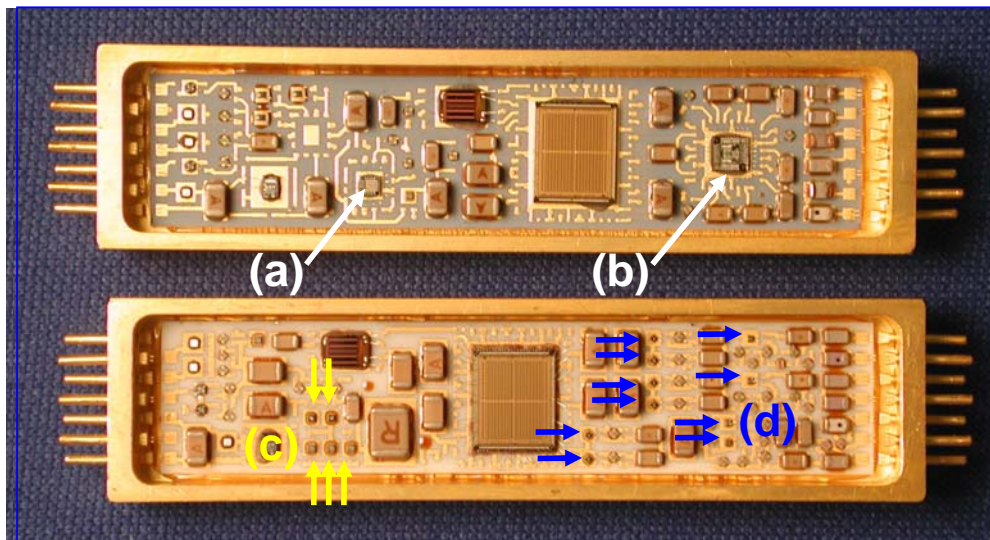


Figure 5. Equivalent circuits: The top circuit uses a transistor array (a) and an ASIC (b) to replace 15 discrete transistors used in the previous version (c) and (d) respectively.

Big caps and inductors are better left outside

While integrated circuits benefit from increased reliability and smaller space when packaged in a hybrid assembly, other components do not. Placing large passive components inside a hybrid forces the package size and cost up, while driving overall circuit reliability down. Conversely, taking these components out of the hybrid increases pin-count, increases the number of external interconnects and adds complexity to the total system design. The relative benefits of each solution must be weighed carefully before implementing a particular hybrid design. For ultimate reliability, eliminating such components altogether may be the best solution.

It is well known that tantalum and electrolytic capacitors have limited life at high temperatures. Tantalum typically fairs better, but the wet-slug versions (Figure 6-a) have been known to dry out and solid versions (Figure 6-b) may become conductive as they are exposed to elevated temperatures for extended periods of time. Placing these devices inside a hybrid would yield no benefit to the component, and would subject the remaining components and interconnections within the hybrid to harmful out-gassing by-products. While there are several companies who are working on high-density capacitors for high temperature, we are not aware of any commercially available high-density capacitors small enough to fit in a reasonable hybrid package. Even large-value X7R ceramic capacitors can be

problematic (Figure 6-c). Package sizes greater than 3 mm are likely to become detached due to either TCE mismatches in thermal-cycled environments or because of their relatively large mass in high shock environments.

In many cases, surface mount designers tend to over-size and over-use capacitors because they are cheap and reliable. In hybrid designs where space and reliability is critical, a careful analysis is in order so that capacitors are right-sized for the application. In many cases, a smaller bypass capacitor will yield improved performance over larger values because of better high frequency characteristics. Also, shorter traces and better ground-plane coupling on ceramic substrates can reduce the requirements of the bypass capacitors. Clever circuit design can often further reduce capacitor requirements.

We have some experience with small-valued inductors (Figure 6-d). If constructed properly, these may be appropriately packaged within a hybrid. Considerations are the Curie temperature of the core material if it is not ceramic, the wire insulation temperature rating, and for bobbin-type inductors, the attach method between the bobbin and its substrate. Encapsulated inductors are not usually appropriate, however, since the encapsulation materials tend to degrade with time at temperature. Large power inductors are usually best left outside of the hybrid since incorporating them inside would increase the package and substrate size and cost significantly.



Figure 6. Capacitors (left to right): (a) wet-slug tantalum, (b) dry tantalum, (c) multilayer ceramic (NPO, X7R), and (d) ferrite bobbin inductor.

Resistors are OK to a point

Low-power resistors are readily available for hybrids. We have had very good success with both thick-film and metal film resistors. Thick-film resistors may be printed directly on the substrate; they are less expensive than metal film and have increased ESD immunity because of the thicker materials. On the down side, they have poorer initial tolerance and a higher temperature coefficient. Metal-film resistors are more susceptible to ESD because of the thin conductor traces. We have also seen significant yield issues with large-valued resistors (150k Ω and greater) built on the smallest ceramic resistor packages (0202). It is best not to use the extreme values in a given package size even though the vendor may offer such devices (this is true for any passive device, not just resistors). Careful consideration must be given to high-power or high-voltage resistors. In many cases these are more appropriately left outside of the package because of the large dimensions involved.

A common pitfall is trying to use extremely large resistors in high temperature circuits. Leakage currents in integrated circuits and capacitors increase exponentially with temperature. Bias currents set by large-valued resistors may be swamped by high leakage currents as temperatures push up to 200°C and beyond. A 1 M Ω pull-up resistor is ineffective if the total leakage current into the attached gates exceeds a few micro amps; using a 10M Ω resistor with a 1 μ F capacitor in an integrator will not yield the desired results when the effective capacitor leakage resistance also approaches 10 M Ω . Micro power and high temperature are rarely compatible.

Simple is better

Every connection is an opportunity for failure. While redundancy is often used to improve reliability in critical systems, it can also be counter-productive since redundancy also increases complexity, which in turn decreases reliability. The following hypothetical example illustrates this principle. A single transistor is used for a critical function. It has a 10% probability of failure in a non-catastrophic open-circuit mode. By adding a second device in parallel, the probability of system failure due to this device going open-circuit is reduced to 1% (0.1 x 0.1). It would follow that an additional (third) device would change the probability to 0.1%. However, in adding two extra devices, we have also added 6 interconnections which might have a 0.5% probability of failure in a catastrophic mode where one failure could take down the entire system. With 9 of these interconnects in the system, the probability of system failure has increased to 4.5% for the second, catastrophic failure mode. While the first redundant device was beneficial, the second redundant device actually made things worse. Admittedly, the example is contrived, but the point remains valid:

common sense must be used. Is it better to add a protection diode or not? The answer depends on whether the likelihood of a failure being prevented by the presence of the diode is more than the likelihood that the diode itself will become a failure mode.

Conclusions

While the benefits of hybrid packaging technology for high temperature applications have been known for many years, the use of this technology has been limited until recently. Availability of high temperature components has been a major issue. Recent initiatives have improved the supply situation, but more needs to be done in this arena. The choice of integrated circuits remains limited and we are aware of no large-value capacitors ($>1\mu\text{F}$) that are commercially available in hybrid compatible packages. A basic understanding of the limits of the technology can lead to better circuit design for hybridization: while some components benefit from hybrid packaging, others are best left outside or avoided completely. Simplicity generally leads to higher reliability so eliminating unnecessary complexity from the design will generally improve reliability. When properly designed, a hybrid circuit can be built to reliably withstand up to 3000 hours at 250°C.

References

- [1] M. Watts, "Empirical Study of High Temperature Circuit Reliability", Proceedings of the International Conference on High Temperature Electronics, Oslo, Norway, June 5-8, 2001 pp. 23-30.
- [2] M. Watts, "Life Testing of High Temperature Electronic Circuits for Down-hole", Proceedings of the 2004 IMAPS International Conference and Exhibition on High Temperature Electronics (HiTec 2004).
- [3] M. Watts, "High Temperature Circuit Reliability Testing", Proceedings of the International Conference on High Temperature Electronics, Paris, France, 2005.
- [4] Arvind Chandrasekaran, "Effect of Encapsulant on High-Temperature Reliability of the Gold Wirebond-Aluminium Bondpad Interface", University of Maryland, Master of Science Thesis, 2003.
- [5] F. P. McCluskey, R. Grzybowski, T. Podlesak, "High Temperature Electronics", CRC Press, New York, 1997, pp. 149-153.
- [6] A. Teverovsky, "High-Temperature Degradation of Wire Bonds in Plastic Encapsulated Microcircuits", 15th European Microelectronics and Packaging Conference & Exhibition (EMPC 2005).
- [7] A. Teverovsky, "Effect of vacuum on high-temperature degradation of gold/aluminum wire bonds in PEMs," 42nd Annual IRPS 2004, pp.547-556.
- [8] L. Demeüs, L. Vancaillie, V. Dessard, and G. Picún, "Ultra Low-Power 10-bit A/D Converter for Harsh Environments", HITEC 2006, May 2006, Santa Fe, USA
- [9] B. Ohme, M. Larson, J. Riekels, S. Schlesinger, K. Vignarajah, and M. Ericson, "Progress Update on Honeywell's Deep Trek High Temperature Electronics Project", HITEC 2006, May 2006, Santa Fe, USA
- [10] S. Rose, "A 225°C Rated ASIC for Quartz Based Downhole Transducers," High Temperature Electronics Conference, Oxford, England, 2007.