High Temperature CMOS Reliability and Drift

Shane Rose
Quartzdyne Inc.
4334 W. Links Drive
Salt Lake City, Utah 84120
Phone: (801)-266-6958 Fax: (801) 266-7985

Abstract

Quartzdyne precision pressure transducers are required to continuously operate at 200°C for more than 5 years (>1 year at 225°C). Future electronics are targeted for 250°C operation. The current transducer electronics are based on 3 custom ASICs; an Oscillator, Voltage Regulator and a Frequency counter. Understanding custom integrated circuit component drift and interconnect life at temperature is crucial for the next generation of sensor applications.

In this study, basic components are aged under bias at 225°C, 250°C and 275°C. Components include P-FET transistors, polysilicon resistors, and a diode connected PNP transistor. Measured parameter drift versus temperature and electrical stress is used to estimate device drift over time. Measured voltage regulator drift is compared with estimated drift based on resistor and diode measurements.

Standard aluminum circuit interconnect life is measured at 3 current densities and temperatures. A modified current density guide is derived from Black's equation. Measured circuit interconnect life is shown to increase when diffusion barriers are present. Powered Quartzdyne hybrid circuit life results at 225°C are compared to expected lifetimes.

Key words: CMOS Reliability, ASIC, Voltage Regulator, High Temperature Electronics,

Introduction

Quartzdyne transducer electronics are based on 3 custom CMOS ASIC's, an Oscillator, Voltage Regulator and a Frequency counter. Quartzdyne pressure transducers are required to operate a minimum of 5 years at 200°C (1 year at 225°C). Future generations of transducers are targeting 250°C operation.

The survivability of these devices has been shown through powered life testing and lifecycle testing. The powered life test system powers the transducer in a 225°C oven, while measuring its outputs daily. Lifecycle testing is un-powered aging at 250°C with 15 Temperature cycles per week, followed by periodic functional testing.

ASIC component drift at 3 temperatures and under electrical bias is studied. Three basic devices, P-FET transistors, polysilicon resistors, a diode connected PNP transistor are aged thermally and electrically. Interconnect life is estimated; an estimated current density guideline is shown. Trace life is extended by diffusion barriers.

Mid range polysilicon resistors show -6% drift at 225°C & 1900hrs, at 250°C their drift is less predictable. The high value polysilicon resistors drift direction and magnitude is not consistent. Aged parts drifted ±4% off their initial values after 1500hrs. The 250°C limited diode data shows I_s (Saturation Current) and ΔV_d drift. The Voltage Regulator output is estimated using measured diode curves and resistor drift data. The estimated regulator output drift bottoms out at -23mV (.9%). The measured Voltage Regulator drift and estimated drift both show a positive step due to an unintended temperature cycle.

P-FET transistor aging is worst case -10% after 1300hrs of 225°C aging. The transistors show a large initial shift and followed a linear drift rate throughout the test. Results at higher temperatures are similar, except that the drift rate decreases until it's approximately constant at 275°C. Both drift rate and offset are greater for shorter channel devices and higher bias voltages.

Measured circuit interconnect life is longer than expected. Interconnect aging shows diffusion barriers extend life. Trace resistance tends to slowly increase with a diffusion barrier rather than suddenly fail without one.

Test Configuration

Test devices are mounted in hybrid modules, wire bonded and sealed up. The modules are soldered to high temperature cables and mounted in glass pans and placed in ovens set to 225°C, 250°C and 275°C. All devices are aged powered for the duration of the test. Power is removed briefly to take device measurements.

Unfortunately, many of the devices show signs of ESD damage both visually and electrically. Only the remaining resistors and diodes that behave normally and exhibit no visual signs of ESD damage are reported on. Transistor modules use 9.1V zener diodes to protect both the gate and the drain from ESD damage. Using this hybrid configuration, zener diode construction prevents N-FET ESD protection.

Polysilicon Resistor Drift

Resistors are essential to filters, bias generators, voltage references, and many more circuits. Performance drift of these circuits affects the overall IC circuit functionality and useful life. Two types of polysilicon resistors are aged; Table 1 describes the test conditions. The lowest bias level simulates the typical operating conditions of the voltage regulator ASIC. Both devices are 50µm X 5µm, producing resistors with about 1.3KΩ for a mid range (Poly-M) and 12kΩ for the high resistive type (Poly-H).

Table 1 Resistor Configurations

Temp.	Poly-H (1.2kΩ/□)	POLY-M (130Ω/□)	Units
225°C	35	70	µA/µm
250°C	7,35, &140	14,70 &140	µA/µm
275°C	35	70	µA/µm

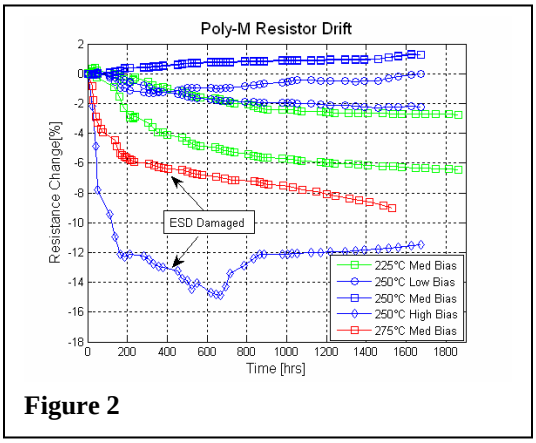

Figure 2

Figure 2 shows the measured poly-m resistor drift. At 225°C the drift is fairly consistent in direction and shape. After 1000hrs, the drift rate decreases to approximately 0.1%/wk. A continuation of this trend leads to about 5.2%/yr drift rate.

The 250°C drift results are less predictable. Two parts drift positive during most of the test, one part changed direction, and the remaining part drifted mostly negative. The positive drifting parts have the highest bias current. The final interesting note is that these parts drifted less than their 225°C equivalents. Unfortunately, the only 275°C and one 250°C functioning resistors have visible ESD damage. The initial measurements are 15%-25% high; these two parts drifted at a faster rate and towards their nominal value.

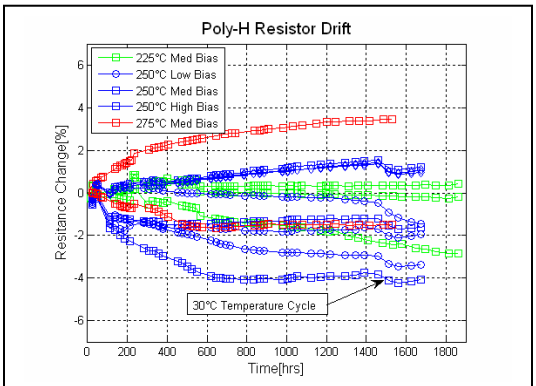

Figure 3

Poly-H resistor drift data are shown in Figure 3. Resistors at all 3 temperatures are inconsistent in direction and magnitude. It is difficult to reasonably predict the drift of these resistors. Near 1450hrs a 30°C temperature cycle occurred, due to a 250°C oven malfunction. All affected resistors show a shift, most of these resistors started recovering by the end of the test.

Diode Drift

The voltage regulator IC uses vertical PNP transistors connected as diodes. Diode connected transistors are aged at 3 bias currents and 250°C. Current-Voltage (I-V) curves provide ΔV_d and I_s at each time step.[1] Due to the ESD issues, the parts meant for the 225°C and 275°C tests are unusable.

The I_s drift is shown in Figure 4. One of the highest biased devices exhibits a 5-6x change in I_s. The remaining devices drift at a much slower rate. The 30°C temperature cycle roughly doubled I_s on all but the worst device, which is not effected. Unlike the resistors, the diodes show no sign of short term recovery.

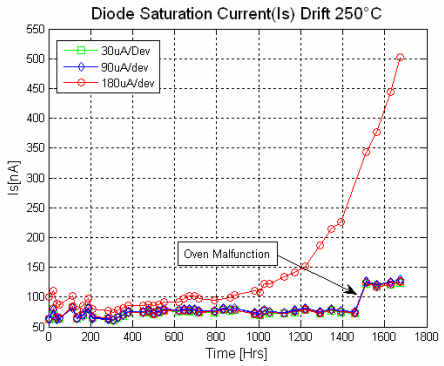

Figure 4

Voltage reference circuits use two diodes biased with different bias currents to generate a constant voltage.[2] This ΔV_d is estimated using the measured I-V curves at each time step. Figure 5 represents the ΔV_d drift of each diode using reasonable bias currents. The temperature cycle results in a 4mV shift of ΔV_d.

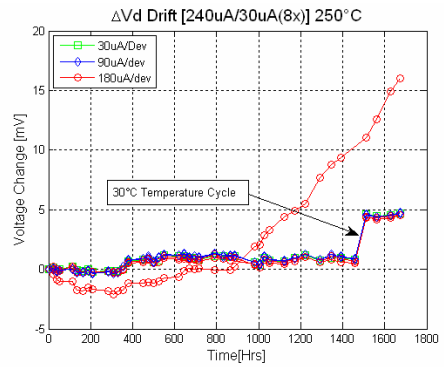

Figure 5

Voltage Regulator Drift

Figure 6 shows 14k hours of 5V biased 225°C powered life data measured on four voltage regulators. The worst case output shift is 0.7% (18mV). Power outages caused two 200°C temperature cycles. The temperature cycles result in a +4mV and +10mV (0.9%) shift on one of the outputs. In both cases the outputs shift back after some time. The first return occurred 1100hrs after the event, the second is 2000hrs after its corresponding event. The second case starts a slow recovery before suddenly shifting down 7mV.

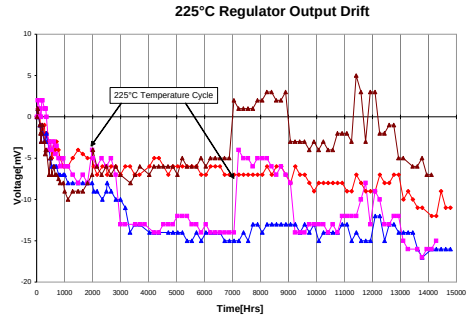

Figure 6

Estimated Voltage Regulator Drift

Using the measured I-V diode curves and resistor drift data, the output of a voltage regulator output is estimated. Equation 1 is used to estimate the voltage output.[2]

Eq. 1 $$V_{reg} = 2\left[I_{ptat}\left(R_1 + R_3\right) + V_{dctat} \right]$$

Eq. 2 $$I_{ptat} = \frac{\Delta Vd}{R_3}$$

Eq. 3 $$R_1 \cong \frac{0.5V_{reg} - V_{dctat}}{I_{ptat}} - R_3$$

R_1 & R_3 are scaled with the Poly-M resistor drift data (Figure 2). At each time step, I_{ptat} is adjusted for the new resistor value. An estimated V_{dctat} is found, and used to calculate V_{reg}. The results for three Poly-M resistor and diode pairs are plotted in Figure 7.

The overall drift ranges from -0.9%(-23mV) to +1.0% (+25mV). The estimated drift also shows the 30°C temperature cycle, as a positive 13-15mV shift. The 225°C measured data shows +10mV shift after a 200°C temperature cycle (Figure 6).

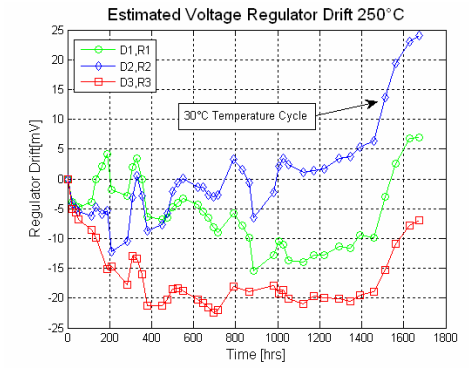

Figure 7

P-Channel MOSFET Drift

The drain and gate of each transistor are shorted together, during the aging and the testing of the devices. A voltage sweep from 0 to 5V using 100mV steps provides data to extract threshold voltage(V_t) and the peak current. The threshold voltage is extracted using the sqrt(I_d) method.[1] The accuracy of V_t measurements at 275°C is limited, due to the low V_t (approx. 250mV). The peak current measured at 2.5V simulates supply voltage of Quartzdyne ASICs. The transistors are aged at higher bias levels to accelerate the test. Table 2 summarizes the quantities and device configurations.

Table 2 P-FET Sample Qty's

Temp.	Bias	W=20µm L=0.8µm	W=40µm L=1.6µm	W=60µm L=3.2µm	W=60µm L=9.6µm
225°C	5V	2	1	2	0
	8V	2	3	2	0
250°C	5V	2	2	2	0
	8V	3	1	0	2
275°C	5V	2	2	2	0
	8V	2	2	2	0

Both the V_t and peak current measurements can be approximated with an initial offset and linear drift rate after 200hrs. Figures 8 and 9 summarize the results; detailed V_t and peak current drift data is shown in the appendix.

The threshold voltage data show positive drift at 225°C, mostly flat for 250°C and slightly negative for 275°C.

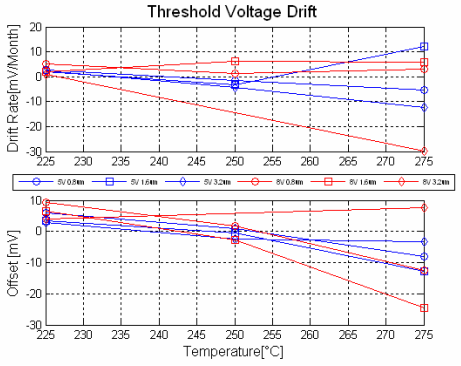

Figure 8

The peak current drift data (Figure 9) shows the initial shift is greater with shorter length transistors and higher voltages. The interesting note is that the drift rate decreases as temperature increases and became positive at 275°C, in some cases.

Over-all there are competing drift mechanisms, one that is positive with electric field and the other is negative with temperature. The two commonly mentioned failure mechanisms for P-FETs are NBTI (Negative Bias Temperature Instability) and hot-carriers. Both mechanisms affect the threshold voltage and saturation current.

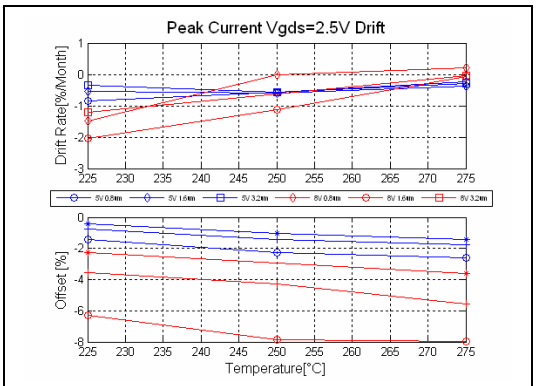

Figure 9

Circuit Interconnect Life

Interconnects are key to long-term high-temperature ASIC life. IC foundry current density guidelines are generally based on a 10-20year life at 125°C. A typical guideline is 1mA/µm but can be 7mA/µm with thick metal options. Electronmigration can be predicted using Black's law (Eq. 4)[3]. By solving for the current density J, and defining a ratio J_{FD}/J_{HT} (Eq. 5), a simple scale factor provides a guideline for high temperature long-term operation. Where J_{FD} is the foundry's guideline and J_{HT} is the modified guideline for high temperature operation.

Eq. 4 $$MTTF = \frac{A}{J^2}\exp\left[\frac{Ea}{kT}\right]$$

Eq. 5 $$\frac{J_{FD}}{J_{HT}} = \sqrt{\frac{MTTF_{HT}}{MTTF_{FD}}\exp\left[\frac{Ea}{k}\left(\frac{1}{T_{FD}}-\frac{1}{T_{HT}}\right)\right]}$$

Figure 10 shows the scale factor (J_{FD}/J_{HT}) vs. target lifetime for 3 cases. Products targeting 5yrs at 225°C life should follow a 0.2-0.3mA/µm guideline. Products that require 200°C and 5yrs should scale the foundry guideline down approximately 2.5 times.

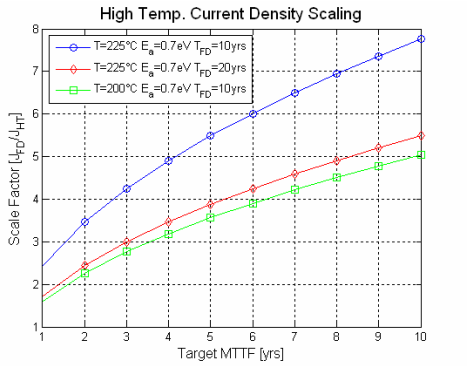

Figure 10

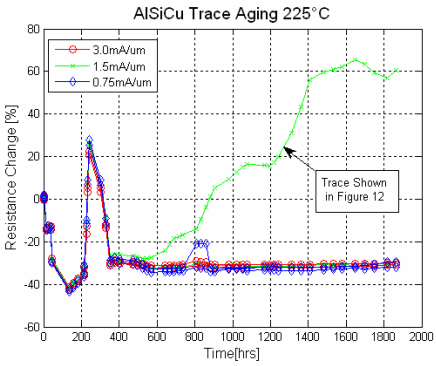

Figure 11

To verify this guideline, metal traces are aged at 3 temperatures and 3 current densities for more than 1500hrs. Devices are biased with 5V and a series resistor chosen to provide the desired current densities. The current densities are designed to produce failures around 250-850hrs at the highest bias level, see Table 3 for details.

Table 3 Expected Trace MTTF

Temp.	W=2µm L=155µm	W=4µm L=156µm	W=8µm L=90µm
225°C	3.0mA/µm	1.5mA/µm	0.75mA/µm
	250hrs	600hrs	2500hrs
250°C	1.4mA/µm	0.7mA/µm	0.35mA/µm
	500hrs	1350hrs	5350hrs
275°C	0.75mA/µm	0.38mA/µm	0.19mA/µm
	850hrs	2250hrs	9000hrs

Resistance measurements are shown in Figures 11, 13 and 14. Initial resistance measurements are inaccurate; as shown by the large swing in figure 11. At 375hrs, the system was adjusted to measure resistance via the slope of an I-V curve, rather than a single point. Subsequent measurements are more consistent. The data in Figures 13 & 14 were obtained after this change and are not subject to the same error shown in Figure 11.

At 225°C the total test time is 7.6x the MTTF, at 250°C this ratio is 3.2, at 275°C it is 1.8. The length of the 225°C test and the lack of failures at 3.0mA/µm suggest that either the 0.7eV activation energy, or the estimated foundry target lifetime may be low. The only failure overall was at 225°C and 1.5mA/µm; Figure 12 shows the failed trace.

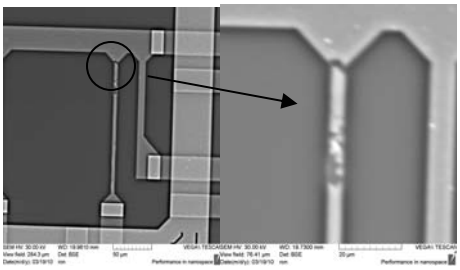

Figure 12

The electronmigration wear on this trace is clear, including an apparent void. In this state, the trace measures approximately 18Ω; the diffusion barrier under the AlSiCu metallization is providing the connection. Presence of the diffusion barrier was verified using Energy Dispersive X-Ray Spectroscopy.

Because diffusion barriers are highly resistive to electronmigration, circuit life can be extended.[4] As the standard AlSiCu trace is worn down by electronmigration, the current shifts to the diffusion barrier. Over time, the trace will tend to increase its resistance followed by circuit performance decay. Without the diffusion barrier, the circuit will fail more abruptly and sooner.

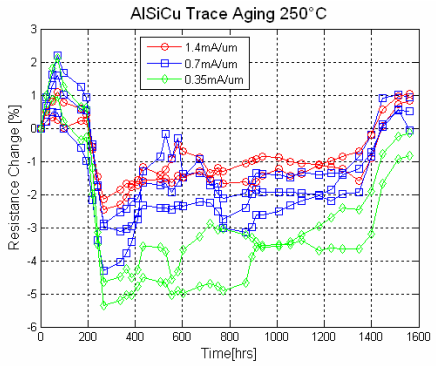

Figure 13

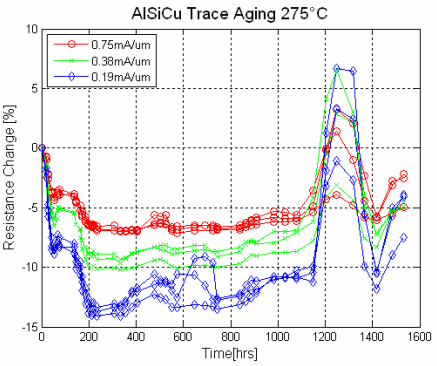

Figure 14

Conclusion

In preparation for 250°C Quartzdyne transducers, custom ASIC component drift is studied. Aged mid-range polysilicon resistors show a -6% shift after 1900hrs of biased aging at 225°C, while showing less drift at 250°C. Higher value resistor drift data are not consistent in direction and magnitude. Poly-H resistors drifted ±4%, during a 1600hrs electrically biased test up to 275°C.

Aged diode-connected PNP transistor I-V curves along with resistor drift data are used to estimate voltage regulator drift at 250°C. Estimated drift shows similar temperature cycle induced shifts as the directly measured results.

Overall estimated voltage regulator drift ranged from -23mV to +25mV after 1700hrs at 250°C. The 225°C measured voltage regulator drift shows a -18mV drift after 14000hrs. A comparison of the estimated and measured results suggests drift accelerates 8-9x for every 25°C increase in temperature. If this holds true, drift at 200°C should be around 2-3mV after 14000hrs.

P-FET aging can be approximated with a simple initial offset and linear drift rate. Initial offsets are large compared to drift rates for all studied transistor lengths. The largest offsets are seen on the 0.8µm devices biased at 8V. Counter to intuition, drift rates change sign with increasing temperature. The peak current drift rates at 225°C are negative, 250°C is mostly flat and at 275°C drift rates can be slightly positive. The Vt drift rates at 225°C are positive, 250°C is mostly flat and at 275°C is slightly negative.

Circuit interconnect life of common AlSiCu traces life can be extended by a diffusion barrier. The diffusion barrier acts as a higher resistive backup connection. Circuit traces with diffusion barriers tend to increase resistance over time, rather than abruptly disconnecting. The result is longer circuit life than predicted by simple electronmigration.

Bulk silicon ASIC development for operation at 250°C is possible. However, ASIC component drift must be considered in the development process. ASIC designers must also consider circuit trace construction and layout to achieve the desired life.

Acknowledgements

The author would like to thank Terry Nielson for the numerous measurements, Muris Beslagic for building the hybrid test modules, Trang Dang for soldering cables to the modules, and Ron Smith for SEM pictures and diffusion barrier verification.

References

[1] Richard S. Muller, Theodore I. Kamins “Device Electronics for Integrated Circuits”, John Wiley & Sons, 1986

[2] David Johns, & Ken Martin “Analog Integrated Circuit Design”, John Wiley & Sons, 1997

[3] Black J.R. “Electronmigration-A Brief survey and some recent results”, IEEE trans Electron Devices

[4] F. Wei, C. Gan, C. Thompson, et all, “Length Effects on the Reliability of Dual Damascene Cu Interconnects”

[5] Pect, Micheal. “The Influence of Temperature on Integrated Circuit Failure Mechanisms.”, Quality and Reliability Engineering International, May-June 1992, Vol. 8, No 3, pp.167-175.

[6] Rose Shane, Watts Mark, “Quartzdyne ASIC Developments”, HITEN 2009 (www.quartzdyne.com)

[7] Rose Shane. “A 225°C Rated ASIC for Quartz based Downhole Transducers” HITEN 2007, (www.quartzdyne.com)

Appendix

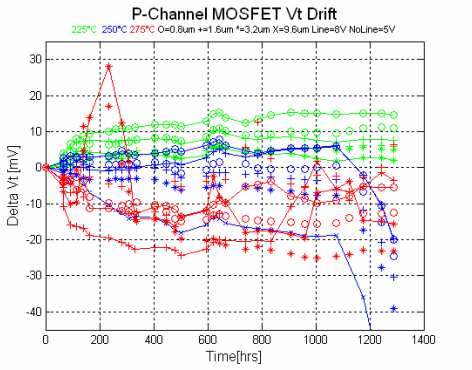

Figure 15

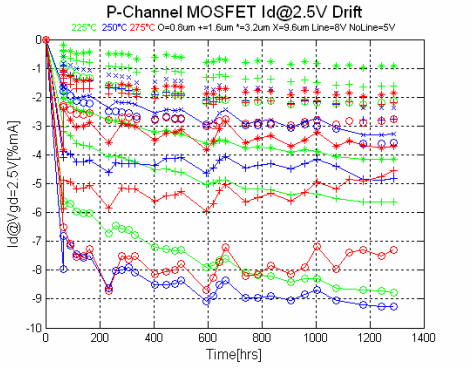

Figure 16