Life Testing of High Temperature Electronic Circuits for Downhole

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Abstract

We present updated results of continued testing of high temperature electronic circuits. Particular emphasis is placed on hybrid circuits tested at 225°C where nearly 1 million device test hours have been logged each of the last three years. Weaknesses in the component attachment have been identified. When processed optimally, the polyimide attachment materials perform well for high temperature and high vibration deployment. A significant number of units, however do not perform to acceptable levels. The conductive polyimide process is highly sensitive to process variations, resulting in reduced reliability. Using thermal cycling followed by high impact shock testing we are able to adequately screen marginal units. This process tests both component attachment and wire bond integrity. Additionally, alternate materials are being investigated to reduce the process sensitivity. These alternate materials allow testing to 250°C and above.

Introduction

Quartzdyne manufactures precision quartz pressure transducers sold primarily to the downhole oil and gas service industry. This market demands high reliability under extreme temperature and vibration conditions. Historic problems with circuits supplied by outside "experts" brought to our attention the importance of in-house testing and qualification. In an effort to improve the quality and reliability of our product, we initiated a test plan for all of our production circuits. Over time, the test results have allowed us to compare different processes, vendors, and circuit technologies, and to identify and address the weak links. The test results also provide a baseline from which expected field life under typical conditions can be predicted.

Results of this ongoing test have been reported earlier [1], [2]. While the complete test results will be summarized, this paper will focus primarily on recent observations specific to the hybrid circuit.

Oscillator Circuit

Each circuit consists of three oscillators, two mixers, CMOS output drivers, and a regulator. Active components include discrete transistors, small transistor arrays, CMOS inverters, and a voltage reference. The circuit is dominated by passive components, including approximately 25 resistors, 30 ceramic capacitors, and up to 2 inductors. Total operating power is less than 50mW. Figure 1 is a photograph of circuits typical of those tested. A digital version of the circuit is also included in the tests. The digital circuit replaces the mixers and output drivers with a field programmable gate array (FPGA) which implements the mixers, a frequency counter and a communications protocol.

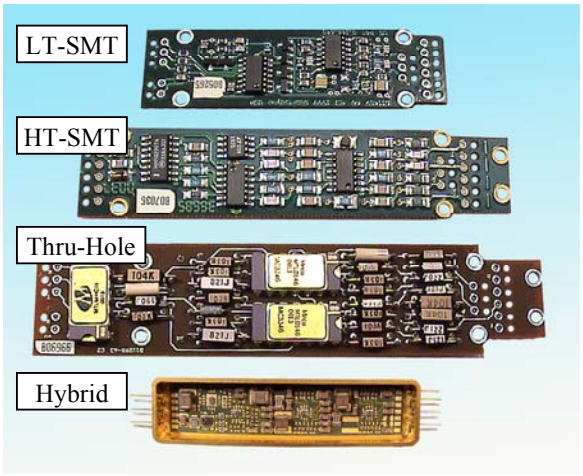

Figure 1. Photograph of boards typical of test units.

Circuit Technologies

The Low-Temperature Surface Mount circuit (LT-SMT) uses commercially available surface mount components and processes. Passive devices include 0805 and 1206 chip resistors and ceramic chip capacitors (NPO, X7R). Active devices are packaged in SOIC or SOT packages. The substrate is a four-layer polyimide board with components on both sides. Plating is hot air leveled SnPb over Ni-plated

Cu traces. Boards are re-flowed using a nitrogen-filled convection oven. The Digital Surface Mount (DL-SMT) uses the same technology as the LT-SMT, with the addition of the 100-pin TQFP packaged FPGA.

The High-Temperature Surface Mount circuit (HT-SMT) uses the same components as the LT-SMT except that SOT packages are not used. Board plating is NiPdAu over copper. SnPb plated leads are double-dipped in SnAg solder to remove Pb. Components are attached using CASTIN®, a variant of SnAg solder produced by AIM [3]. Soldering is done by hand on a hot plate with strict solder-temperature control. Some of the more recent boards in this category were built by Innova Electronics, Inc. using Innovalloy® solder [4]. There is no difference in the performance of the two groups in these tests.

The Thru-Hole circuit uses custom through-hole components specifically designed for high temperature use. Resistors are epoxy-encapsulated metal-film rated to 275°C. Capacitors are ceramic packaged with High Melting Point PbSnAg (HMP) lead terminations. Active devices are custom-packaged in brazed lid ceramic packages. The PCB substrate is polyimide, with fused SnPb over Ni plated copper. HMP solder is used in a hand process, which includes a hot plate, and careful temperature control tailored to the individual package types. Due to space constraints, this oscillator does not include a regulator.

The Hybrid circuit uses an alumina substrate with doped Au conductors [5]. Conductive and non-conductive polyimides are used for component and die-attach. Select devices are attached using eutectic solder. Wire bonding incorporates both Au and Al wires based on the die metalization [6]. The substrate is packaged in a custom seam-welded metal package, which includes mounting holes. External wiring is direct to the Hybrid package. No circuit boards are used in the product.

Test Procedure

A significant percentage of every lot of circuits built by or for us is destructively tested. The test (Life/Cycle) includes a mixture of time at temperature and thermal cycling. Some units are also subject to high frequency vibration or shock testing. To simplify testing, units are not powered during the test. This is justified by the very low power consumption of the circuit under normal operation, and has been validated by powered tests done on a smaller sample size.

Time at temperature and thermal cycling are accomplished using forced-air convection ovens running continuously at 150°C, 180°C, 200°C, and 225°C. Samples are left in the ovens over night and weekends. Each working day, the samples are removed from the ovens and allowed to cool to room temperature for approximately 30 minutes, after which they are returned to the ovens for a minimum of one hour. The process is repeated such that each sample gets 15 thermal cycles and 160 hours of time at temperature each week. Every two weeks the units are tested electrically.

Figure 2. Hybrid Circuits in Life/Cycle test being cycled to ambient temperature.

Surface mount units are also subjected to ultrasonic vibration to expose weakening solder joints. For the hybrid units, a portion of the test sample is subjected to high-impact shock testing. The test is a 1-meter free-fall with a metal-to-metal impact, repeated 25 times. The impact is not instrumented, as we have not found an accelerometer capable of surviving this test. We estimate the impact to be approximately 1 million g's in 1 microsecond based on extrapolation of data measured at lower impacts. This sequence is repeated biweekly until 100 drops have accumulated. The Thru-Hole boards are not subject to shock or vibration testing. We know that the Thru-Hole design is not mechanically robust, and do not recommend it for high-shock applications.

We have found that the combination of tests described is much more effective than the same tests performed separately. Our first attempts at independent aging, thermal cycling, and shock and vibration testing did not expose faults that were obvious when boards were subject to normal use. Each portion of the test suite is the result of identifying a particular failure (either in the field, or during processing), and then searching for a test that exposes that failure mode. Consequently, the tests

have become more severe over time. They are purposely designed to induce failure, rather than mimic typical usage patterns. Prior to 1998, tests were terminated when a milestone lifetime was achieved, as a lot qualification. Beginning in 1998, the test policy was changed such that all circuits are now tested to destruction. Lifetime data in this report is based on tests performed from April 1998 through February 2004.

Test Results

Since 1998, more than 5 million test-hours have been logged on over 1000 circuits. The test matrix is displayed below (Table 1). Note that for each circuit there is a primary temperature where most data has been taken (Table 1-a). Several small-scale tests have been performed at off-temperature points (Table 1-b), but these do not have the statistical significance of the larger tests.

Table 1. Life/Cycle Test Matrix: Primary Tests (a), and Off-Temperature Tests (b)

(a) Test ID	Qty	Hours	MTTF
DL-SMT (150°C)	11	34,248	3,021
LT-SMT (150°C)	172	1,756,224	12,011
HT-SMT (180°C)	462	823,841	1,749
Thru-Hole (200°C)	119	464,438	4,033
Hybrid (225°C)	292	1,940,141	7,362
Total	**1056**	**5,018,892**	

(b) Test ID	Qty	Hours	MTTF
LT-SMT (180°C)	2	3,600	1,800
HT-SMT (150°C)	2	38,100	19,050
HT-SMT (200°C)	2	1,392	696
Thru-Hole (150°C)	1	23,304	23,304
Thru-Hole (180°C)	1	6,648	6,648
Thru-Hole (225°C)	2	1,520	760
Total	**10**	**74,564**	

Plotting the survival rate of the primary tests versus test time at each observed failure yields the plot in Figure 3. The smoothed lines on the graph are a best-fit Weibull model [7], [8]. The average time to 90%, 50%, and 10% failure are calculated from the smoothed function. Ideally, the survival rate would stay high initially, and then drop quickly as the wear-out mechanism begins to dominate. The hybrid line shows the lowest slope or broadest distribution, indicating that random, rather than wear-out failures dominate its survival rate [9].

In Figure 4, the mean time to failure (MTTF) for each of the test points has been plotted versus the test temperature. Error bars are shown at the 10% and 90% mean failure times. In addition, the commonly used 2x/10°C de-rating curve has been plotted to give an indication of possible de-rating. While the off-prime points are not statistically significant, it can be seen that this de-rating is at least reasonable for these devices. Future tests will be designed to establish better de-rating models.

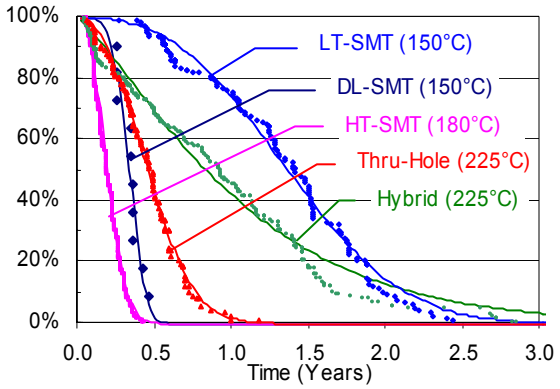

Figure 3. Survival Rate plotted at each failure time. Smooth lines are best-fit Weibull Survival Function.

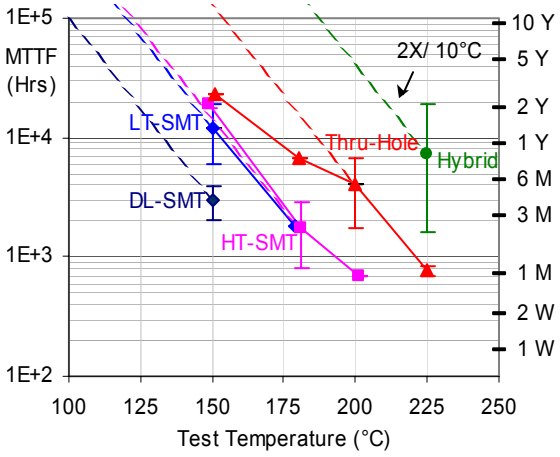

Figure 4. Mean Time to Failure (MTTF) for various circuit technologies in Life/Cycle test. Error Bars at 10% and 90%. Nominal de-rating of 2X/10°C is shown for reference. The non-linearity of the Thru-Hole points suggests multiple independent failure mechanisms.

The HT-SMT and LT-SMT projections are quite close to each other. This is consistent with the failure mechanism in each case being independent of the solder process. In both cases, the primary failure mode is wire-bond breakdown that has been accelerated by SOT and SOIC package decomposition [10], [11]. This tends to occur more quickly in the smaller SOT packages. For this reason, the SOT package is not used with the HT-SMT. The limiting failure mode of the DL-SMT

circuit is conductivity through the decomposed plastic between adjacent pins of the 100-pin TQFP package that is used in this circuit. The lead-frame spacing on the TQFP is significantly smaller than on the SOIC packages in the other designs, explaining the shorter life of approximately four months at 150°C. It is hoped that higher temperature plastics developed as part of the Pb-free initiatives may soon be available that will improve the high-temperature performance of these commercial SMT devices.

The custom packaging and higher melting point solder used in the Thru-Hole provides almost an order of magnitude improvement over the surface mount technologies. This is at the expense of size and ruggedness. The Thru-Hole circuits cannot tolerate the ultrasonic vibration or high-impact shock to which the surface mount and hybrid assemblies are subjected. Note that at lower temperatures, the Thru-Hole test does not follow the 2X/10°C de-rating. It is suspected that thermal cycling and handling are more significant factors in these tests than is time at temperature. The 150°C Thru-Hole board saw 2008 thermal cycles in 23,304 hours. Performance in a non-cycled powered test is significantly better at the lower temperatures, and follows the 2X/10°C projection much more closely (14,000 hrs at 180°C, and 35,000+ hrs at 150°C). Because of the success of the Hybrid circuit, the Thru-Hole circuit is no longer offered by Quartzdyne. All Life/Cycle testing of this circuit technology has been completed.

Hybrid Failure Mode Analysis

The Hybrid results clearly demonstrate an advantage over the other technologies. The mean and upper limits for the Hybrid are stable, and not likely to increase appreciably with the present technology. We are pushing the wear-out limits of the conductive component attachment at 1-2 years. On the other hand, the lower 10% failure limit of just over 2 months at 225°C is disappointing. We believe that it can be improved significantly, and work is under way to accomplish this.

In Figure 5 the test hours for each hybrid unit is plotted versus the date the unit was initially put into test. Units which have failed are marked with an "**X**"; units still surviving, with an open triangle (**Δ**). Key process changes are identified along the top of the graph (a-f). There are a significant number of units with failure times well below the average life. The limiting failure mode for these early failures is identified on the graph. It can be seen that there is an obvious grouping of the failure modes. This grouping is also clear in Figure 6 where the percentage of each failure mode for *all* failures is plotted versus date of manufacture.

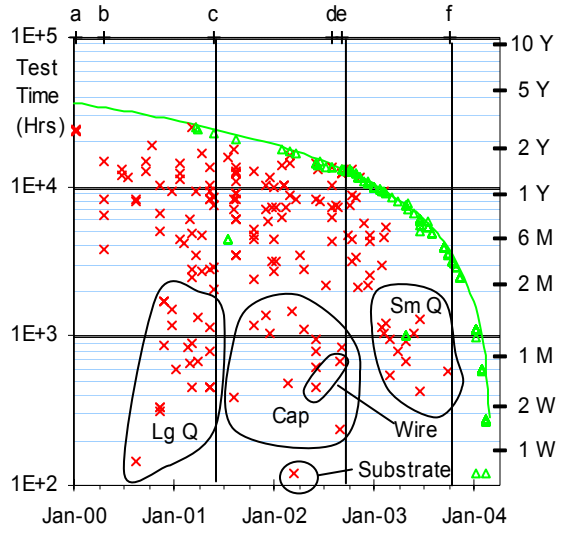

Figure 5. Test times for production hybrid units in Life/Cycle test. Failed units are denoted with an "X"; open triangles "Δ" indicate units still surviving. The latter generally follow the elapsed time line until failure. Dominant failure modes are indicated for early failures. Key process changes are are identified by letter: a) initial prototypes, b) first production units, c) eutectic attachment for large transistors, d) process change for cap and substrate attach, e) 100% drop screen, and f) eutectic attach for small transistors.

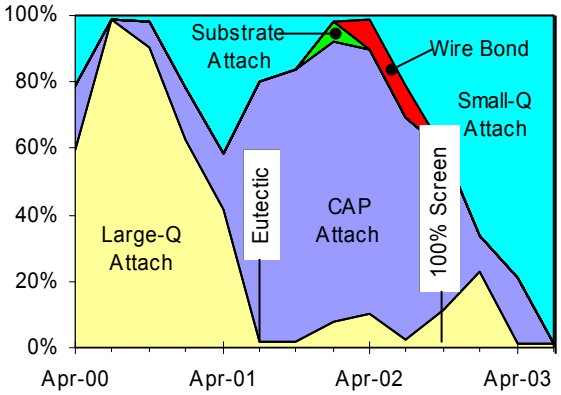

Figure 6. Dominant Life/Cycle failure modes versus time. Includes both infantile and end of life failures. Significant process changes are also noted.

The first four prototypes survived nearly 24,000 hours with a very tight distribution (Figure 5-a). The first batch of production units showed a much broader distribution with an average of 8200 hours (Figure 5-b). In our experience, it is not uncommon for initial prototypes to behave better than production units given the care and attention payed to these units.

The first significant problem to appear was a high-impedance collector-to-substrate connection on a large transistor used in the regulator (Lg-Q). As this problem became more prevelant, a solution was identified. In May of 2001, the conductive polyimide used to attach these components was replaced with a eutectic solder (Figure 5-c). This solution completely eliminated infantile failures of this class. The few failures of this class shown in Figure 6 in 2002 and 2003 are related to the eutectic attachment and occurred at approximately 8,000 hours.

The next significant failure mode was breakdown of the conductive polyimide used to attach capacitors (Cap). This failure mode was much more random than the transistor problem. One particular lot had an initial failure at 384 hours, while the other units in the same lot lasted 7,000 and 18,000 hours respectively. The problem appeared to be related to process variation rather than a fundemental limit of the materials. Several attempts were made to address the issue which was finally resolved with a series of process changes implemented in August 2002 (Figure 5-d).

Two additional problems are indicated in the graphs during this time frame: a poorly attached substrate (Substrate) and some marginal wirebonds (Wire). The substrate attach problem was completely solved by a process change. A 100% high-impact drop screen was implemented in September 2002 (Figure 5-e) which effectively screened for the wirebond problem. This screen is also effective at exposing marginal substrate and capacitor attachment problems. By screening 100% of all units we not only increase our confidence, but are able to provide timely feedback to the vendor, allowing them to respond to problems earlier. We presently see very few failures in the initial screen.

A failure mode involving a pair of small transistors has now become significant (Sm-Q). As shown in Figure 6, the failure mode existed as early as April 2000 at a low level. Only now that the other problems have been reduced is it revealing itself as the remaining dominant failure mode. It is the same failure mode that the larger transistors showed, but the circuit is less sensitive to it in the smaller transistors. We expect that the eutectic attachment solution used on the larger transistors will be similarly effective on the smaller ones. This change was implemented in September of 2003 (Figure 5-f). No early failures have been oberved since this change was implemented.

It should be noted that the three dominant failure modes are all related to the conductive polyimide used for component attachment. We are presently working on a process in our in-house hybrid facility that eliminates this material. Preliminary samples on test coupons have been tested at 250°C and showed good results up to 5000 hours. The process development is nearly complete and we expect functioning units in test shortly.

Field Life

Figure 7 shows the field return rates for hybrid circuits produced over the last three years [12]. The return rates are in line with Life/Cycle Test early failure rates, and process improvements driven by the Life/Cycle testing have been effective in reducing the overall return rate. That being said, the correlation between test and field failures is less than perfect.

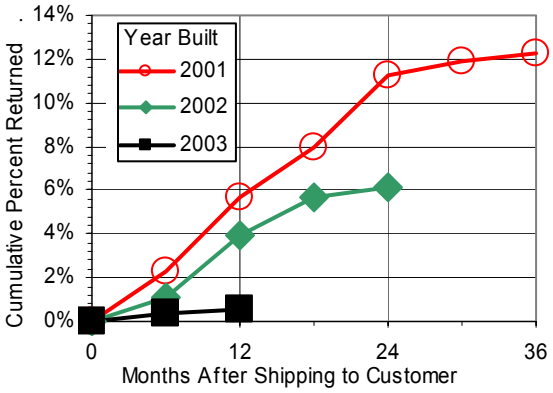

Figure 7. Cumulative customer return rate for Hybrid circuits. The last two points of each series may still rise as the periods are not yet closed.

Figure 8 compares the percent of field failures with Life/Cycle failures for each failure mode. It is clear that the failure distribution is not the same in the field as in the Life/Cycle test. Substrate detachment (SUB) and broken wire-bond (WIRE) categories are much more frequent in the field than in in-house testing. Once these failure modes were identified, the process changes and screens discussed earlier were initiated to address them. No parts manufactured with the new process have failed in the field for substrate detachment. We expect the field return rate to remain low for units now shipping.

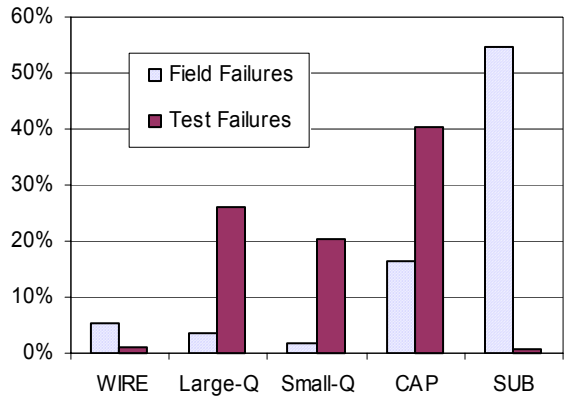

Figure 8. Comparison of Field Failures to Life/Cycle Test Failures. While substrate detachment (SUB) is the most prominent field failure, it has been observed only once in Life/Cycle testing. Other failure modes show better correlation.

Conclusion

Servicing the down-hole oil and gas market requires extreme vigilance in order to provide the highest quality products possible. When pushing the limits of components and materials it is important to continually monitor the process, identify weak links, and work towards improving the product. The following pseudo-code illustrates this:

```
While (in business) {
        Build it the best you know how.
        Test it to death.
        Learn how to make it better.
}.
```

Acknowledgements

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