

High Temperature Circuit Reliability Testing

Updated March, 2005

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Abstract

As a manufacturer of pressure transducers designed for high temperature use, we have found that providing circuits to survive the rigors of high temperature and high shock environments requires constant vigilance. The results of an ongoing study comprising over ten years of testing circuits are presented. These tests include over six million test hours on 1190 circuit assemblies. Circuit technologies tested include surface mount, through-hole, and hybrid assemblies. Both frequency-output and digital-output oscillator circuits have been tested. The testing consists of time at elevated temperature, as well as thermal cycles distributed over the duration of the test. Some tests also include periodic high frequency shock and vibration. All circuits are tested to failure. The tests have become more severe over time in order to better expose weaknesses as these have been discovered. Recent test results have shown a significant increase in expected lifetimes for hybrid assemblies, while surface mount lifetimes have declined. The reasons for these changes are discussed.

1. Introduction

Quartzdyne manufactures precision quartz pressure transducers sold primarily to the upstream oil and gas service industry. In order to assure the quality of the product that we sell, we have established a test procedure for all of our production circuits. The test results are used to qualify circuit assembly lots, and to provide valuable input in order to improve our process. Over time, the test results have allowed us to compare different processes, vendors, and circuit technologies, and to identify and address the weak links. The test results also provide a baseline from which field life can be predicted. Results of these tests have been presented earlier [1], [2]. The focus of this update is on lessons learned in the last 1-2 years of testing.

2. Oscillator Circuit

Each circuit consists of three oscillators, two mixers, CMOS output drivers, and a regulator. Active components include discrete transistors, small transistor arrays, CMOS inverters, and a voltage reference. The circuit is dominated by passive components, including approximately 25 resistors, 30 ceramic capacitors, and up to 2 inductors. Total operating power is less than 50mW. Figure 1 is a photograph of circuits typical of those tested. A digital version of the circuit is also included in the tests. The digital circuit replaces the mixers and output drivers with a field programmable gate array (FPGA) which implements the mixers, a frequency counter and a communications protocol.

Circuit Technologies

The Low-Temperature Surface Mount circuit (LT-SMT) uses commercially available surface mount components and processes. Passive devices include 0805 and 1206 chip resistors and ceramic chip capacitors (NPO, X7R). Active devices are packaged in SOIC or SOT packages. The substrate is a four-layer polyimide board. Plating is hot air levelled SnPb over Ni-plated Cu traces. Boards are re-flowed using a nitrogen-filled convection oven. Hand rework is not allowed. The Digital Surface Mount (DL-SMT) uses the same technology as the LT-SMT, with the addition of the 100-pin TQFP packaged FPGA.

The High-Temperature Surface Mount circuit (HT-SMT) uses the same components as the LT-SMT with the exception that SOT packages are not used. Board plating is NiPdAu over copper. SnPb plated leads are double-dipped in SnAg solder to remove Pb. Components are attached using CASTIN®, a variant of SnAg solder produced by AIM [3]. Soldering is done by hand on a hot plate with strict solder-temperature control. Some of the more recent boards in this category were built by Innova Electronics, Inc. using Innovalloy® solder [4]. There is no difference in the performance of the two groups in these tests. Because of the short life of plastic packages, HT-SMT is no longer offered by Quartzdyne.

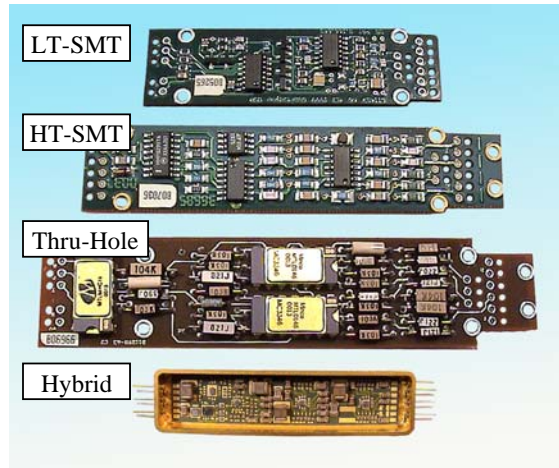


Figure 1. Oscillator Circuits Tested

The Thru-Hole circuit uses custom through-hole components specifically designed for high temperature use. Resistors are epoxy-encapsulated metal film rated to 275°C. Capacitors are ceramic packaged with High Melting Point PbSnAg (HMP) lead terminations. Active devices are custom-packaged in braised lid ceramic packages. The PCB substrate is polyimide, with fused SnPb over Ni over copper. HMP solder is used in a hand process, which includes a hot plate, and careful temperature control tailored to the individual package types. Due to space constraints, this oscillator does not include a regulator. This technology is no longer used by Quartzdyne.

The Hybrid circuit uses an alumina substrate with doped Au conductors [5]. Conductive and non-conductive polyimides are used for component and die-attach. Select devices are attached using eutectic solder. Wire bonding incorporates both Au and Al wires based on the die metallization [6]. The substrate is packaged in a custom seam-welded metal package. External wiring is direct to the Hybrid package. No circuit boards are used in the product.

Because of reliability issues, inductors are no longer used in standard product. They are used for reworking older transducers where quartz compatibility issues dictate.

3. Test Procedure

A percentage of every lot of circuits built by or for us is destructively tested. The test (Life/Cycle) includes a mixture of time at temperature and thermal cycling. Some units are also subject to high frequency vibration or shock testing. To simplify testing, units are not powered during the test. This is justified by the very low power consumption of the circuit under normal operation, and has been validated by testing a smaller number of circuits in continuously powered tests.

Time at temperature and thermal cycling are accomplished using forced-air ovens running continuously at the maximum test temperature for each technology. Samples are left in the ovens over night and on weekends. Each working day, the samples are removed from the ovens and allowed to cool to room temperature for approximately 30 minutes, after which they are returned to the ovens for a minimum of one hour. The process is repeated such that each sample gets 15 thermal cycles and 160

hours of time at temperature each week. The units are tested electrically at ambient temperature every two to four weeks.

Surface mount units are also subjected to ultrasonic vibration to expose weakening solder joints. For the hybrid units, a portion of the test sample is subjected to high-impact shock testing. The test is a 10-40 inch free-fall with a metal-to-metal impact, repeated 25 times. The impact is not instrumented, as we have not found an accelerometer capable of surviving this test. We estimate the impact to be approximately 1 million g's in 1 microsecond based on extrapolation of data measured at lower impacts. This sequence is repeated biweekly until 100 drops have accumulated. The Thru-Hole boards are not subject to shock or vibration testing. We know that the Thru-Hole design is not mechanically robust, and have never recommend it for high-shock applications.

We have found that the combination of tests described is much more effective than the same tests performed separately. Our first attempts at independent ageing, thermal cycling, and shock and vibration testing did not expose faults that were obvious when boards were subject to normal use. Each portion of the test suite is the result of identifying a particular failure (either in the field, or during processing), and then searching for a test that exposes that failure mode. Consequently, the tests have become more severe over time. Prior to 1998, tests were terminated when a milestone lifetime was achieved, as a lot qualification. Beginning in 1998, in response to market pressures for longer circuit lifetimes, the policy was changed such that the test circuits are now tested to destruction. Lifetime data in this report is based on tests performed from April 1998 through January 2005.

4. Test Results

Since 1998, nearly 6.5 million test-hours have been logged on 1190 circuits. The test matrix is displayed below (Table 1). For each circuit there is a primary temperature where most of the data has been taken. Several small-scale tests have also been performed at off-temperature points, but these do not have the statistical significance of the larger tests.

Table 1. Life/Cycle Test Matrix: Primary Tests are Highlighted

Test ID	Qty	Test Hours	MTTF
DL-SMT (150°C)	23	75,450	3,026
LT-SMT (150°C)	190	1,862,822	6,008
LT-SMT (180°C)	2	3,600	1,800
HT-SMT (150°C)	2	38,100	19,050
HT-SMT (180°C)	475	831,266	552
HT-SMT (200°C)	2	1,392	696
Thru-Hole (150°C)	1	23,304	23,304
Thru-Hole (180°C)	1	6,648	6,648
Thru-Hole (200°C)	119	464,438	4,033
Thru-Hole (225°C)	2	1,520	760
Hybrid (225°C)	370	3,148,887	30,911
Hybrid (250°C)	3	16,553	5,518
Total	1190	6,473,980	

Plotting the survival rate of the primary tests versus test time at each observed failure yields the plot in Figure 2. Each point is calculated as the number of units that have survived at least that long divided by that total plus all prior failures. The smoothed lines on the graph are a best-fit Weibull survival model [7], [8]. From the smoothed lines we can predict time to failure based on all of the data points in the test. Figure 3 is essentially the same plot as Figure 2, except that the data set is limited to parts manufactured in the last eighteen months. The survival rate based on 6 years of data is also plotted in Figure 3 as dashed lines for reference.

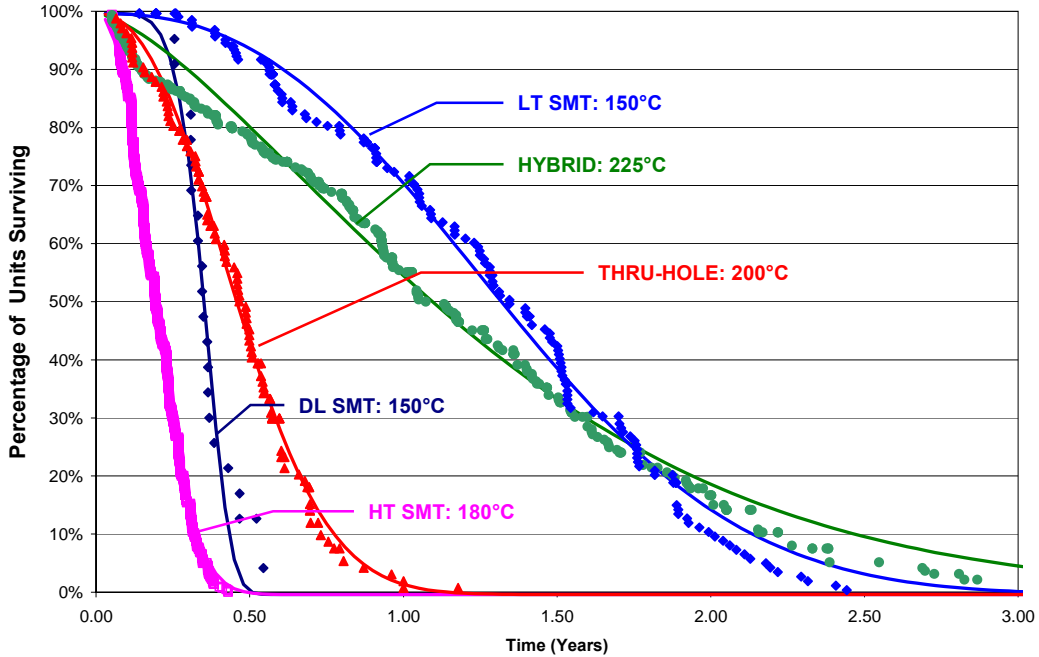


Figure 2. Survival Rate plotted at each failure time for primary test temperatures. Smooth lines are best-fit Weibull Survival Function based on testing from April 1998 through January 2005.

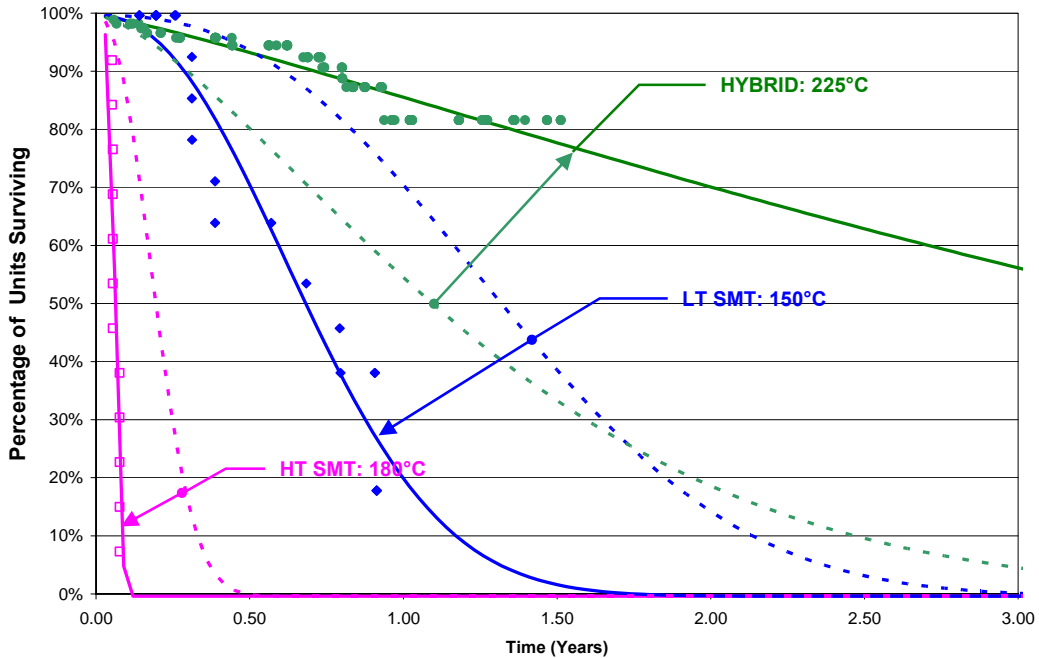


Figure 3. Survival Rate plotted at each failure time for last 1.5 years only (July 2003 through January 2005). Solid lines are best-fit Weibull survival function for 1.5 year data. Dashed lines are from 6 year data. Note the improvement in Hybrids, while SMT technologies have become worse. The Hybrid projection may be optimistic because the end-of-life wear-out mechanism has not yet been observed.

The projections are clearly different for the recent data, indicating a significant change in process life. The surface mount units have seen a significant decline in lifetimes, while the Hybrid shows substantial improvement. Because of the limited data set, we suspect that the long term projections for the Hybrid are somewhat optimistic. These changes will be discussed separately for the SMT and Hybrid technologies.

Reduction in life for SMT assemblies

As can be seen in Figure 3, the lifetime for both of the SMT technologies has dropped in half. This can be explained by recent industry trends towards using plastic IC encapsulants with higher Bromine content. Bromine halogens are commonly used as a flame retardant. At high temperatures these break down and accelerate corrosion of the Au-Al wire bond. The higher Bromine content, coupled with other related resin changes has been shown to decrease the life of the wire bonds at temperatures above 125°C [9]. Fortunately, the European Directive on Hazardous Substances in Electrical and Electronic Equipment (RoHS) calls for a ban on certain brominated flame-retardants by 2006. Electronics manufactures have responded by developing bromine-free encapsulants which could improve lifetimes of SMT packages by as much as four times. Results of preliminary tests on bromine free FPGA packages are very promising. We have zero failures in this package after 6000 hours (2 units) and we are working towards switching all of our SMT plastic components to the newer package type.

Hybrid Failure Mode Analysis

While the Hybrid test results demonstrate a clear advantage over the other technologies, Figure 2 also shows a high number of early failures and a broad distribution of failure times for those Hybrids. This is indicative of a process that is not in complete control. A tighter process would yield a survival function that stayed high initially, and then dropped off steeply as the wear-out mechanism began to dominate. As can be seen in Figure 3, the units built in the last 1.5 years are significantly better than earlier units, showing a much higher early survival rate. An analysis of the failure modes and process changes over the past several years will help to explain the change.

In Figure 4 the test hours for each hybrid unit is plotted versus the date the unit was initially put into test (manufactured). Units which have failed are marked with an "x"; units still surviving, with an open triangle (Δ). Key process changes are identified along the top of the graph. Failure modes are indicated by various symbols and labels as shown in the key. It can be seen that there is an obvious grouping of early failure modes which correlate with the process changes.

The first four prototypes survived nearly 24,000 hours with a very tight distribution. (They appear as a single bold "x".) The first batch of production units showed a much broader distribution with an average of 8200 hours. In our experience, it is not uncommon for initial prototypes to behave better than production units given the care and attention paid to these units.

The first significant problem to appear was a high-impedance collector-to-substrate connection on a large transistor used in the regulator (Lg-Q). As this problem became more prevalent, a solution was identified. In May of 2001, the conductive polyimide used to attach these components was replaced with a eutectic solder. This solution completely eliminated infantile failures of this class. The few failures of this class shown in 2002 and 2003 are related to the eutectic attachment and occurred at approximately 8,000 hours.

The next significant failure mode was breakdown of the conductive polyimide used to attach capacitors (Cap). This failure mode was much more random than the transistor problem. One particular lot had an initial failure at 384 hours, while the other units in the same lot lasted 7,000 and 18,000 hours respectively. The problem appeared to be related to process variation rather than a fundamental limit of the materials. Several attempts were made to address the issue which was finally resolved with a series of process changes implemented in August 2002.

Two additional problems are indicated in the graphs during this time frame: a poorly attached substrate (Substrate) and some marginal wirebonds (Wire). While Life/Cycle test failures for substrate attachment were rare, field failures for this mode were disturbingly high. A 100% high-impact drop screen was implemented in September 2002 which effectively screened for both of these problems. This

screen is also effective at exposing capacitor attachment problems. By screening 100% of all units we not only increase our confidence, but are able to provide timely feedback to the hybrid vendors, allowing them to respond to problems earlier. The substrate attach problem was completely solved by a process change, and we presently see very few failures of any kind in the initial screen.

A failure mode involving a pair of small transistors began to dominate in April 2003 (Sm-Q). As shown, the failure mode existed as early as April 2000 above 3000 hours. Only after the other problems had been reduced did it reveal itself as a dominant failure mode. In fact, it is the same failure mode that the larger transistors showed, but the circuit is less sensitive to it in the smaller transistors. The same eutectic attachment solution used earlier on the larger transistors has been similarly effective on the smaller ones. This change was implemented in September of 2003, and as can be seen from the graph, there have been no failures of this mode since that time.

The only early failures that have been observed since October 2003 are of an inductor that was recently added on a limited number of hybrid units used for repair of old transducers that require it (pre 2000). The inductor is not used in current production, and the failure mode observed in this test has already been resolved.

Now that the typical lifetimes in this test are in the 1-2 year range, we have decided to increase the test temperature to 250°C for new units going into test. It is hoped that this will give more timely feedback on process weaknesses as well as reducing the workload associated with testing so many units for so long. There are presently more than 175 Hybrid units surviving in the 225°C test.

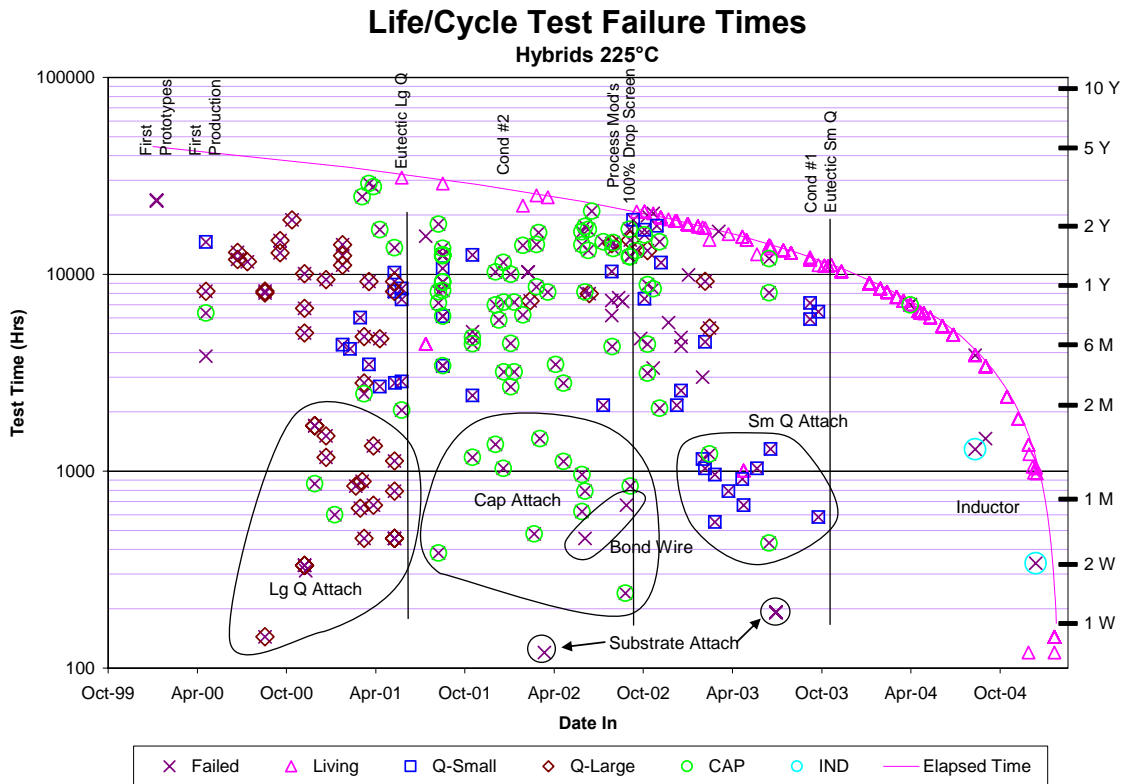


Figure 4. Test times for production hybrid units in Life/Cycle test. Failed units are denoted with an "X"; open triangles "△" indicate units still surviving. The latter generally follow the elapsed time line until failure. Failure modes and key process changes are also identified.

5. Predicting Field Life

Thus far, we have only considered the data at the primary test temperature for each technology. Several small scale tests have been performed at alternate temperatures, and while these may not be statistically significant, they do offer a reasonable de-rating factor. In Figure 5, the time to failure for each of the test points has been plotted versus the test temperature. The time to 50% failure is plotted along with error bars at the 10% and 90% failure times as derived from the Weibull fits described earlier. In addition, the commonly used $2x/10^{\circ}\text{C}$ de-rating curve has been plotted to give an indication of a possible de-rating.

It can be seen that the $2x/10^{\circ}\text{C}$ de-rating is a reasonable approximation for most of the technologies. The exception to this rule is the Hybrid plot where the 250°C data is somewhat higher than would be predicted from just the 225°C data. This can be explained by the process changes discussed earlier. When plotted with data from the just the last 1.5 years (Figure 6), the Hybrid points line up much better, as do the various SMT lines. The Thru-Hole data has been eliminated from Figure 6 since no Thru-Hole circuits have been put into test in the last 1.5 years.

The HT-SMT and LT-SMT projections are quite close to each other. This is consistent with the failure mechanism in each case being independent of the solder process. In both cases, the primary failure mode is wire-bond breakdown that has been accelerated by decomposition of brominated fire retardants in plastic packages [9], [10]. The separation of the DL-SMT from the HT-SMT and LT-SMT projections is misleading in the 6-year data as the latter projections are dominated by the earlier tests. As plastic package composition has changed, the life of all of the surface mount technologies has decreased uniformly.

The ultimate goal of Life/Cycle testing is to provide quality product, along with the information required in order to use that product with confidence. The data presented here is only a starting point towards that end. Actual field life is dependent on the specific environmental stresses to which the product will be subjected. The Life/Cycle tests were originally designed to push the limits of stresses that may be encountered in logging and drilling environments (elevated temperature, rapid thermal cycling and high mechanical shock). Because of the severity of these tests, we would expect field life in a *typical* application to be greater than or equal to the lifetimes predicted by this test data.

In addition to the Life/Cycle testing, we also perform powered life testing at Quartzdyne. This test takes complete transducers, and runs them continually at the maximum temperature. Data from the transducers is monitored, and any anomalies are noted as a failure and analysed. With no thermal cycling, this test more closely matches the conditions typical of a permanent installation. Lifetime in this test is similar to that in life/cycle testing for diffusion related failure mechanisms such as plastic package breakdown. We see longer lifetimes for the Thru-hole and Hybrid technology in this test because the prime failure modes are accelerated by thermal and mechanical shock.

Any projections based on the Life/Cycle data should consider the severity of the actual use environment as compared to the test stresses. Actual field lifetimes may vary significantly, depending on the combination of stress involved. Failure mechanisms are not necessarily the same in the field as those observed in the laboratory due to different mounting conditions and stress levels. Every field failure returned to Quartzdyne is analysed. This information is used as further input for both design improvement and test modification. A full discussion of field reliability of Quartzdyne Transducers is covered in a separate report [11].

Life/Cycle Failure Rate 6-year data updated Jan-2005

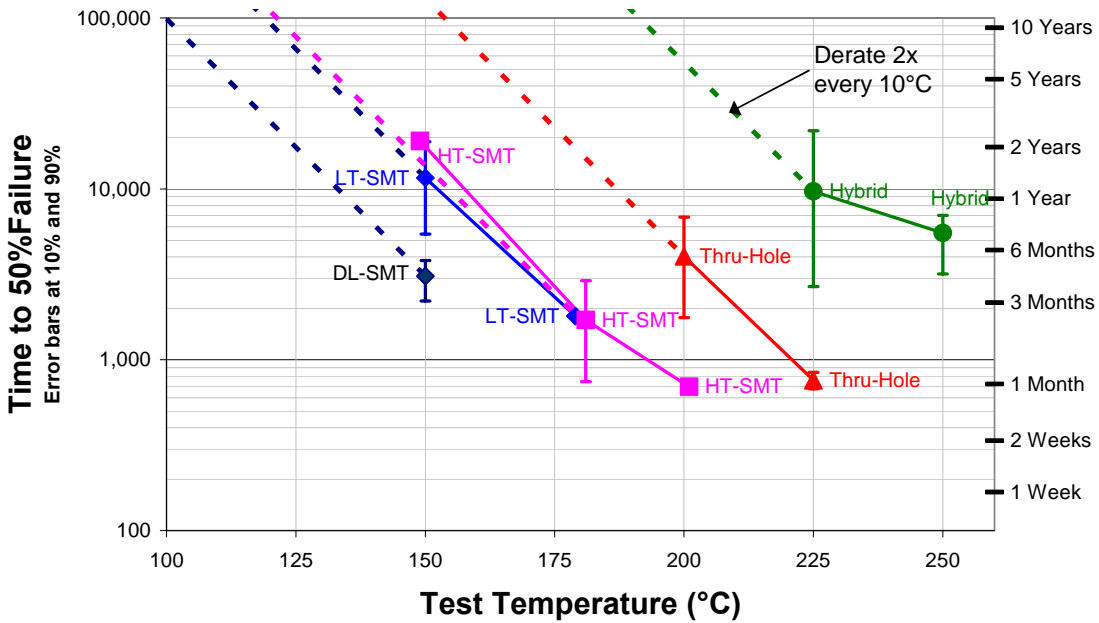


Figure 5. Survival Rate based on 6 years of testing with off-prime tests included. Error bars are at 10% and 90% survival. Nominal de-rating of 2X/10°C is shown for reference.

Life/Cycle Failure Rate 1.5-year data updated Jan-2005

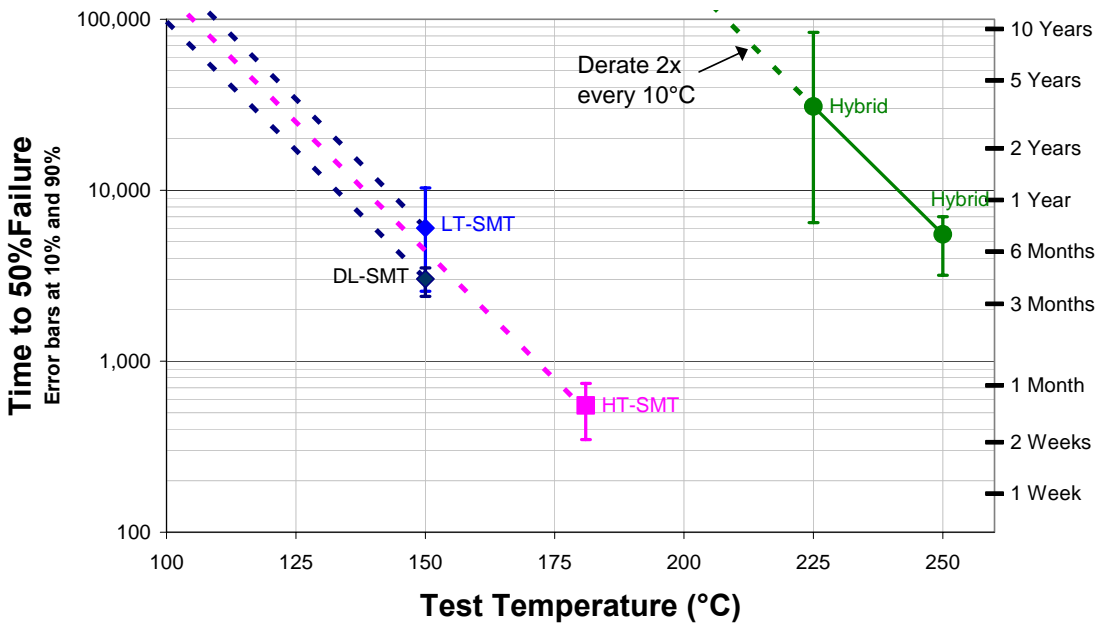


Figure 6. Survival Rates based on last 1.5 years of testing. Error Bars are at 10% and 90%. Nominal de-rating of 2X/10°C is shown for reference.

6. Conclusions

A simple declaration of a maximum operating temperature is not adequate when specifying a product for use in a down-hole environment. Time at temperature, thermal cycling, and shock and vibration are all critical factors in determining circuit life in this hostile environment. Subtle process changes, whether intentional or not can also affect circuit life. Systematic destructive testing is a valuable tool that can be used to monitor quality and to predict useful life of the product.

Surface mount Sn63 with commercially available components and packaging is for applications not exceeding 150°C. Lifetimes of 1 year at temperatures below 125°C can be expected with present plastic packaging in typical down-hole applications. A switch to better plastics is needed to improve these lifetimes to historic levels. Since the limiting factor at these temperatures is package related, rather than solder related, simply switching to exotic solders will not improve the service life.

For temperatures above 150°C, custom packaging is required to achieve lifetimes beyond a few months at temperature. For short excursions up to 200°C, through-hole components can be utilized with appropriately selected components if high shock levels are not expected. For extended time at temperatures above 125°C, carefully constructed hybrid circuit assemblies are preferred. Careful monitoring, and continuous process improvement has yielded a technology that can be used for several years at temperatures up to 200°C, with short-term excursions as high as 250°C.

7. Acknowledgements

The author would like to thank Jacob Li of Vectron International for his help in developing the current Hybrid processes. Thanks also to the management of Quartzdyne for committing the resources required for this testing, and sincere thanks to the electronic technicians at Quartzdyne, for endless hours of circuit testing and analysis.

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