High Temperature Circuit Reliability Testing

Updated February, 2003

Milton Watts
Quartzdyne, Inc.
milt@quartzdyne.com

Abstract

As a manufacturer of pressure transducers designed for high temperature use, we have found that providing circuits to survive the rigors of high temperature and high shock environments requires constant vigilance. The results of an ongoing study comprising over nine years of testing circuits are presented. These tests include nearly four million test hours on 960 circuit assemblies. Circuit technologies tested include surface mount, through-hole, and hybrid assemblies containing commercially available discrete bipolar transistors, small-scale integrated circuits and passive devices. All of the test samples are essentially the same circuit with only minor packaging-driven differences. The testing consists of time at elevated temperature, as well as thermal cycles distributed over the duration of the test. Some tests also include periodic high frequency shock and vibration. All circuits are tested to failure. Based on the test results, it can be concluded that surface mount technology can be used reliably at temperatures as high as 150°C, and up to five years at 125°C. With properly constructed hybrid assemblies, more than two years at 200°C or five years at 180°C can be expected. Since the first release of this paper in June 2001, the number of hybrid units tested has increased significantly, as has our understanding of the limitations of this technology.

1. Introduction

Quartzdyne manufactures precision quartz pressure transducers sold primarily to the upstream oil and gas service industry. In 1994 we experienced widespread circuit failure because we trusted a vendor who claimed to know how to build circuits for downhole applications. While the initial prototypes looked good, the production units received were not of the same quality. Eventually, over 25% of the products shipped with those circuits were returned for circuit failures. In response, we initiated a test plan for all of our production circuits, and used the results of these tests to improve our process. When outside vendors were unable or unwilling to satisfy our ever-increasing demands on circuit technology, we brought the process in house. Over time, the test results have allowed us to compare different processes, vendors, and circuit technologies, and to identify and address the weak links. The test results also provide a baseline from which expected field life under typical conditions can be predicted.

2. Oscillator Circuit

Other than minor packaging-driven differences, the circuits tested are essentially equivalent. Each circuit consists of three oscillators, two mixers, CMOS output drivers, and a regulator. Active components include discrete transistors, small transistor arrays, CMOS inverters, and a voltage reference. The circuit is dominated by passive components, including approximately 25 resistors, 30 ceramic capacitors, and up to 2 inductors. Total operating power is less than 50mW. Figure 1 is a photograph of circuits typical of those tested.

The Low-Temperature Surface Mount circuit (LT-SMT) uses commercially available surface mount components and processes. Passive devices include 0805 and 1206 chip resistors and ceramic chip capacitors (NPO, X7R). Active devices are packaged in SOIC or SOT packages. The substrate is a four-layer polyimide board. Plating is hot air levelled SnPb over Ni-plated Cu traces. Boards are re-flowed using a nitrogen-filled convection oven. Hand rework is not allowed. This process is relatively inexpensive, providing a cost-effective solution for applications to 150°C.

The High-Temperature Surface Mount circuit (HT-SMT) uses the same components as the LT-SMT with the exception that SOT packages are not allowed. Board plating is NiPdAu over copper. SnPb plated leads are double-dipped in SnAg solder to remove Pb. Components are attached using CASTIN®, a variant of SnAg solder produced by AIM. Soldering is done by hand on a hot plate with strict solder-temperature control. Some of the more recent boards from this group were built using a proprietary process provided by Innova Electronics, Inc. While the components are relatively inexpensive, the process costs are high with this technology.

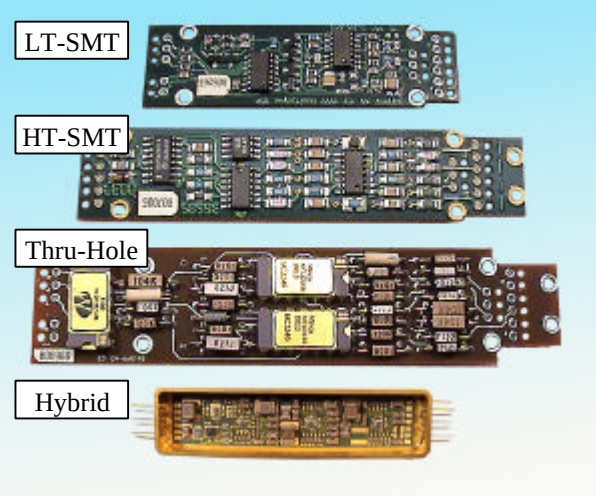

Figure 1. Oscillator Circuits Tested

The Thru-Hole circuit uses custom through-hole components specifically designed for high temperature use. Resistors are epoxy-encapsulated metal film rated to 275°C. Capacitors are ceramic packaged with High Melting Point PbSnAg (HMP) lead terminations. Active devices are custom-packaged in braised lid ceramic packages. The PCB substrate is polyimide, with fused SnPb over Ni over copper. HMP solder is used in a hand process, which includes a hot plate, and careful temperature control tailored to the individual package types. The custom packaged component costs are significantly higher in this technology than in either of the surface mount boards. Processing costs are also high. Due to space constraints, this oscillator does not include a regulator.

The Hybrid circuit uses an alumina substrate with doped Au conductors [1]. Conductive and non-conductive polyimides are used for component and die-attach. Wire bonding incorporates both Au and Al wires based on the die metalization [2]. The substrate is packaged in a custom seam-welded metal package, which includes mounting holes. External wiring is direct to the Hybrid package. No circuit boards are used in the product.

Because of continued reliability problems with the inductors, the Hybrid, and the more recent low-temperature surface-mount circuits have been designed such that the inductors are no longer necessary.

3. Test Procedure

A significant percentage of every lot of circuits built by or for us is destructively tested. The test (Life/Cycle) includes a mixture of time at temperature and thermal cycling. Some units are also subject to high frequency vibration or shock testing. To simplify testing, units are not powered during the test. This is justified by the very low power consumption of the circuit under normal operation, and has been validated by powered tests done on a smaller scale.

Time at temperature and thermal cycling are accomplished using forced-air ovens running continuously at 150°C, 180°C, 200°C, and 225°C. Samples are left in the ovens over night and weekends. Each working day, the samples are removed from the ovens and allowed to cool to room temperature for approximately 30 minutes, after which they are returned to the ovens for a minimum of one hour. The process is repeated such that each sample gets 15 thermal cycles and 160 hours of time at temperature each week. Every two weeks the units are tested electrically. For surface mount units, the units are also subjected to ultrasonic vibration to expose weakening solder joints. For the hybrid units, a portion of the test sample is subjected to high-impact shock testing. The test is a 1-meter free-fall with a metal-to-metal impact repeated 25 times initially, and again after two weeks of exposure to temperature. This sequence is repeated until 100 drops have accumulated (approx. 1000 hrs). The Thru-Hole boards are not subject to shock or vibration testing. We know that the Thru-Hole design is not mechanically robust, and do not recommend it for high-shock applications.

We have found that the combination of tests described is much more effective than the same tests performed separately. Our first attempts at independent ageing, thermal cycling, and shock and vibration testing did not expose faults that were obvious when boards were subject to normal use. Each portion of the test suite is the result of identifying a particular failure (either in the field, or during processing), and then searching for a test that exposes that failure mode. Consequently, the tests have become more severe over time. Prior to 1998, tests were terminated when a milestone lifetime was achieved, as a lot qualification. Beginning in 1998, in response to market pressures for

longer circuit lifetimes, the test policy was changed such that all circuits are now tested to destruction. Lifetime data in this report is based on tests performed from April 1998 through January 2003. Technology improvements are based on the entire 9 years of testing.

4. Test Driven Process Improvements

Table 1 summarises process improvements made since 1994 to improve the lifetime of circuits in the Life/Cycle test for the various circuit technologies. Whenever a failure is observed, whether in process, in destructive testing, or from the field, it is analysed. If a pattern of similar failures is observed, the tests, components, and processes are evaluated, and corrective actions are taken. Full component-level lot tracking allows vendor lot related problems to be identified. If a lot related problem is found, the entire lot can be scrapped from inventory, or recalled if necessary.

The table also lists present limitations of each process. In the LT-SMT circuits, the limiting failure mode of wire-bonds in plastic SOT and SOIC packages [2][3] is deemed an acceptable end-of-life failure and no further action is being taken. In the case of the HT-SMT and Thru-Hole technologies, Quartzdyne has made the decision to retire the technology rather than investing additional resources into extending the lifetimes. For the Hybrid circuit, we are actively pursuing alternate component and substrate attachment technologies to improve the long-term reliability of the circuit.

Table 1. Summary of Process Improvements

Process	Historic Failures	Process Changes	Current Limitations
LT- SMT	- Poor Wetting - SOIC Damage - Cracked Components	- Inspection to identify poor plating. - Nitrogen convection rather than IR re-flow - No hand rework	- Wire bonds in SOT and SOIC packages
HT-SMT	- Solder Breakdown - SOT Wire Bonds - Cracked Components - Molded Inductors	- Inspection to identify poor plating - Add Cu and Sb to solder - Use SOIC instead of SOT packages - Hand solder process tailored to each component type - Use custom open-bobbin inductor	- Wire bonds in SOIC packages - Inductor wire damage
Thru-Hole	- Lid separation of frit-sealed ceramic packages - Wire bonds failure in plastic DIP and TO-18 packages - Lead separation in resistors and capacitors - Poor solder wetting	- Custom ceramic packaging with braised lid for all semiconductors - 260°C rated all-ceramic capacitors - 275°C rated metal film resistors - Solder-dip components for plating compatibility - Hand solder process tailored to each component type	- Capacitor lead separation - Inductor epoxy breakdown - Polyimide substrate breakdown
Hybrid	- Substrate-to-package attachment - Wire bond failure - Component attachment failure	- Substrate and component attachment materials and process changes - 100% screen to detect weak connections	- Polyimide component attach - Intermetallic formation

5. Failure Rates Observed in Testing

The failure rate for each of the standard tests is shown in Figure 2. The failure rate is calculated as the ratio of failed units to total units tested at each point in time [3]. Infantile failures, defined as units that would have been rejected in-house by standard manufacturing tests before being shipped, are not included in the data. The number of units surviving at each sample point is also plotted.

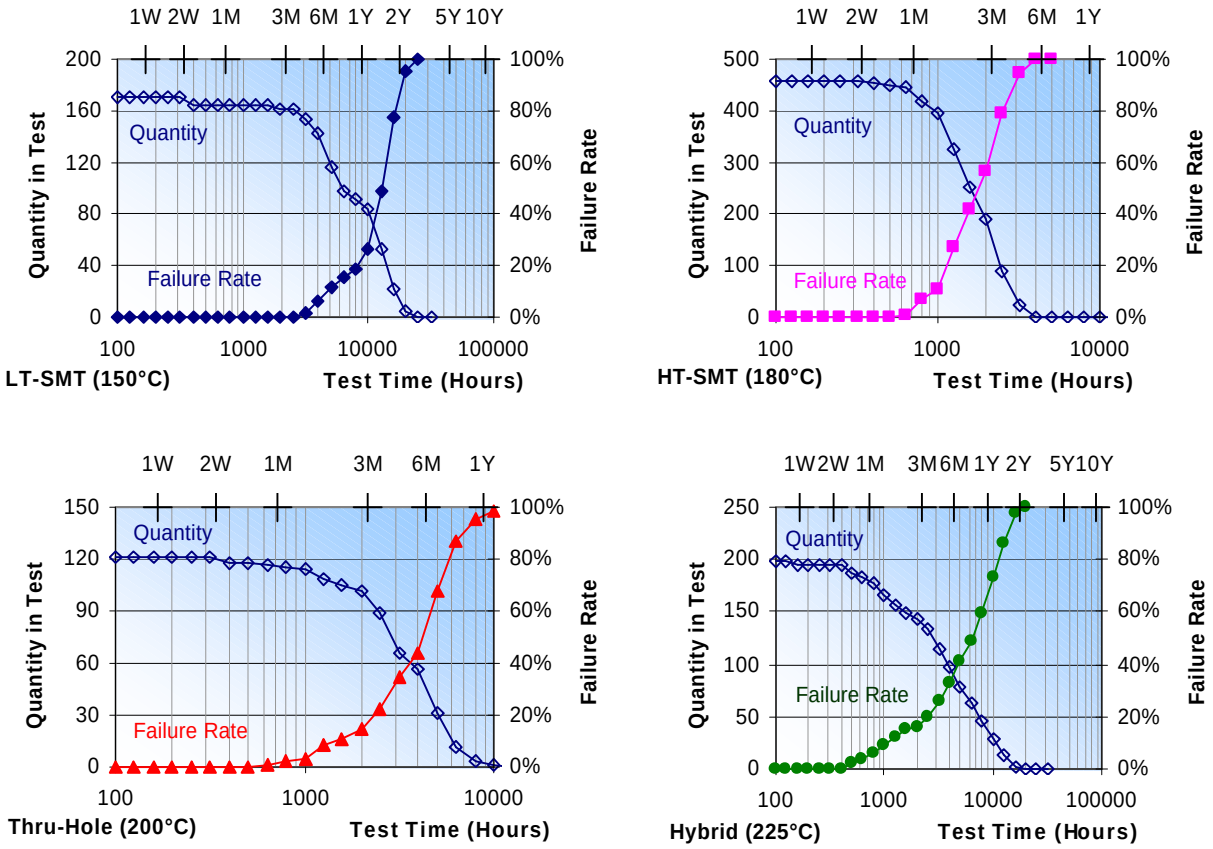

Figure 2. Life/Cycle Failure Rates

Table 1. Number of Samples in Each Test

Technology	Quantity	MTTF	Total Hours
LT-SMT (150°C)	171	12,589	1,592,780
LT-SMT (180°C)	5	1,585	4,464
HT-SMT (150°C)	2	19,953	38,100
HT-SMT (180°C)	457	1,585	816,593
HT-SMT (200°C)	2	631	1,392
Thru-Hole (150°C)	1	19,953	20,064
Thru-Hole (180°C)	1	6,310	6,648
Thru-Hole (200°C)	121	3,981	458,382
Thru-Hole (225°C)	2	794	1,520
Hybrid (225°C)	203	6,310	996,518
TOTAL	**965**		**3,936,461**

While most of the tests have been done at a single, standard temperature for each technology, a limited number of tests have been performed above and below the standard temperatures (). The limited sample size of the non-standard tests does not justify calculation of precise activation energies for the various failure modes. However, it can be seen from the projections in Figure 3, that a nominal factor of two for every 10°C de-rating is at least a reasonable approximation. The 10%, 50%, and 90% failure rate points are plotted as an I-bar.

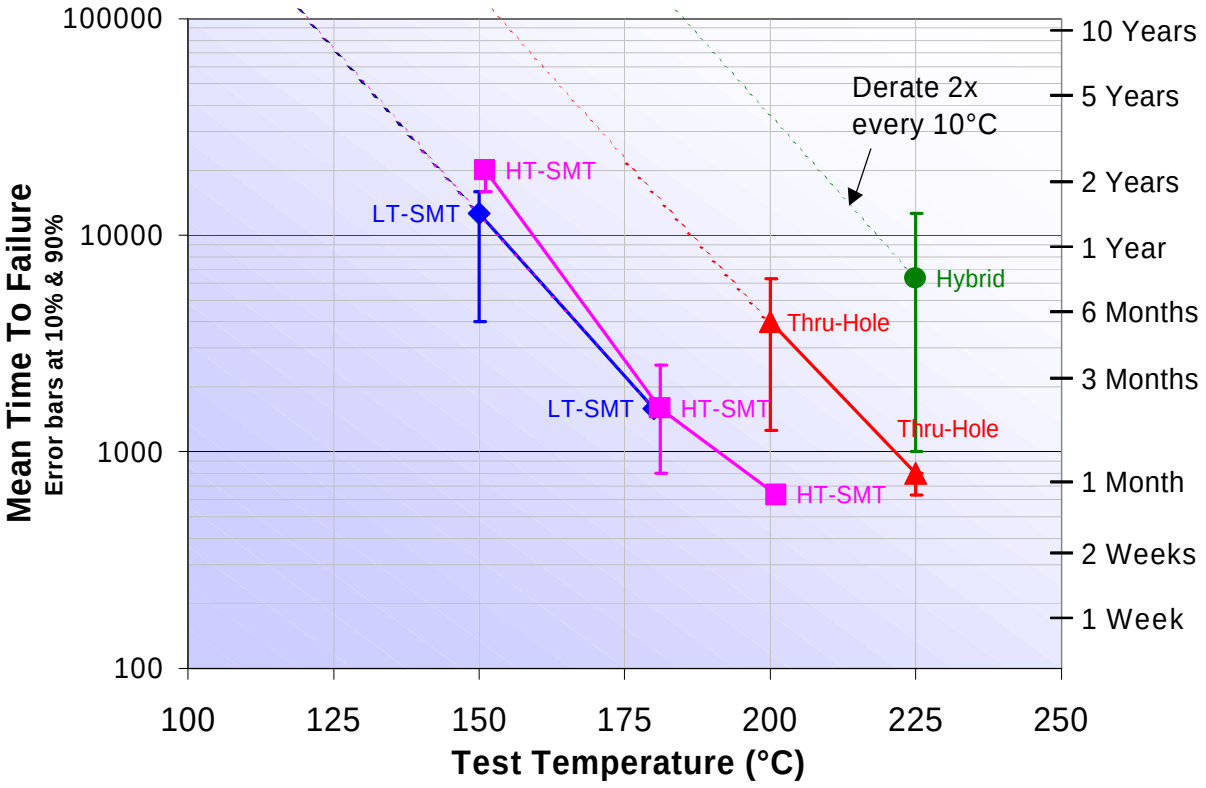

Figure 3 . Life/Cycle Test Derating

Note that the HT-SMT and LT-SMT projections are reasonably close to each other. This is consistent with the failure mechanism in each case being independent of the solder process. In both cases, the prime failure mode is wire-bond breakdown that has been accelerated by SOT and SOIC plastic package decomposition. This tends to occur more quickly in the smaller SOT packages. For this reason, the SOT package is not used with the HT-SMT. Recent tests have confirmed that with fine pitch packages, the limiting failure mode is conductivity through the decomposed plastic between adjacent pins [4]. This occurs at approximately four months at 150°C for a 100-pin TFQP package in our tests.

It can be seen that the custom packaging and higher melting point solder used in the Thru-Hole provides almost an order of magnitude improvement over the two surface mount technologies. This is at the expense of size and ruggedness. The Thru-Hole circuits cannot tolerate the ultrasonic vibration or high-impact shock to which the surface mount and hybrid assemblies are subjected. Because of the success of the Hybrid circuit, the Thru-Hole circuit is no longer in production at Quartzdyne. All testing of this circuit technology has been completed.

The Hybrid results clearly demonstrate an advantage over the other technologies. However, we are not satisfied with the results, particularly the large number of early hybrid failures (10% bar at 1000 hours, 225°C). The primary failure mode has been the conductive polyimide component attachment. We have found that subtle variation in processing, and materials can significantly effect the quality of the joints. We have made both process and material changes to address these failures, and more recent units are showing better consistency.

A second failure mode that we have observed is detachment of the ceramic substrate from the package. Several process changes related to the package and substrate attachment have led to significant improvement in this joint as well. Additionally, we have implemented a 100% screen, which includes 150 hours at 225°C, 15 thermal cycles, and 10 high-impact drops. The screen has effectively eliminated the early failures, and has provided much quicker feedback to the vendor. With these changes, we expect the 10% failure bar to begin rising.

The mean and upper limits for the Hybrid are fairly stable, and not likely to increase with the present technology. At 6-12 months, we are systematically pushing the limits of the conductive polyimide. Improvement beyond this will require eliminating this material. We have identified alternate materials, and have set up a new hybrid production line at our facility that will allow us to do this. Preliminary samples on test coupons are now in test at 250°C and are showing good results after six months.

6. Predicting Field Life

The ultimate goal of Life/Cycle testing is to provide quality product, along with the information required in order to use that product with confidence. The data presented here is only a starting point towards that end. Actual field life is dependent on the specific environmental stresses to which the product will be subjected. The Life/Cycle tests were originally designed to push the limits of stresses that may be encountered in logging and drilling environments (elevated temperature, rapid thermal cycling and high mechanical shock). Because of the severity of these tests, we would expect field life in a *typical* application to be greater than or equal to the lifetimes predicted by this test data.

In addition to the Life/Cycle testing, we are also performing powered life testing at Quartzdyne. This test takes complete transducers, and runs them continually at maximum temperature. Data from the transducers is monitored, and any anomalies are noted as a failure and analysed. With no thermal cycling, this test more closely matches the conditions typical of a permanent installation. Lifetime in this test is similar to that in life/cycle testing for diffusion related failure mechanisms such as plastic package breakdown. For the hybrid technology we are seeing longer lifetimes in this test because the prime failure modes are accelerated by thermal and mechanical shock.

Any projections based on the Life/Cycle data should consider the severity of the use environment as compared to the test stresses. Actual field lifetimes may vary significantly, depending on the combination of stress involved. Failure mechanisms are not necessarily the same in the field as those observed in the laboratory due to different mounting conditions and stress levels. Every field failure returned to Quartzdyne is analysed. This information is used as further input for both design improvement and test modification. A full discussion of field reliability of Quartzdyne Transducers is covered in a separate report [6].

7. Conclusions

A simple declaration of a maximum operating temperature is not adequate when specifying a product for use in a down-hole environment. Time at temperature, thermal cycling, and shock and vibration are all critical factors in determining circuit life in this hostile environment. Systematic destructive testing provides additional information necessary to monitor quality and to predict useful life of the product.

Surface mount Sn63 with commercially available components and packaging is inexpensive, and viable for applications not exceeding 150°C. Lifetimes of 5 years at temperatures below 125°C can be expected in typical downhole applications. Since the limiting factor at these temperatures is package related, rather than solder related, simply switching to exotic solders will not significantly improve the service life.

For temperatures above 150°C, custom packaging is required to achieve lifetimes beyond a few months at temperature. For short excursions up to 200°C, through-hole components can be utilised with appropriately selected components if high shock levels are not expected. For extended time at temperatures above 150°C, carefully constructed hybrid circuit assemblies, which avoid the packaging and circuit board issues associated with conventional technologies, are preferred. With this technology, lifetimes exceeding 5 years at 180°C are possible.

8. Acknowledgements

The author would like to thank Jacob Li and Andy Byk of Vectron International for their help in developing the current Hybrid processes. Also, sincere thanks to the electronic technicians at Quartzdyne, including Mark Hahn, Lisa Chase, Dillon Dwyer, and Lay Lou for endless hours of circuit testing and analysis. Thanks also to the management of Quartzdyne for committing the resources required for this testing.

[1] D. W. Palmer, R. C. Heckman, "Extreme Temperature Range Microelectronics", *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, Vol. CHMT-1, no. 4, December 1978, pp. 333-340.

[2] G. G. Harmon, "Metallurgical Bonding Systems for High-Temperature Electronics", *High Temperature Electronics Edited by R. Kirshcman*, IEEE Press, New Jersey, 1999, pp. 752-769.

[3] F. P. McCluskey, R. Grzybowski, T. Podlesak, *High Temperature Electronics*, CRC Press, New York, 1997, pp. 149-153.

[4] P. McCluskey, Kofi Mensah, C. O'Connor, *Reliability of Commercial PEMs in Extreme Temperature Environments At Elevated Tempeatures*, Fifth International High Temperature Electronics Conference, June 2000.

[5] A. F. Veneruso, A. G. Kosmala, R. Bhavsar, L.J. Bernard, and M. Pecht, "Engineered Reliability for Intelligent Well Systems", *Offshore Technology Conference 2001*, OTC 13031.

[6] L. Perry, *Reliability of Quartzdyne Pressure Transducers*, www.quartzdyne.com, February, 2003.