High Temperature Circuit Reliability Testing

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Abstract

As a manufacturer of pressure transducers designed for high temperature use, we have found that providing circuits to survive the rigors of high temperature and high shock environments requires constant vigilance. The results of an ongoing study comprising over ten years of testing circuits are presented. These tests include over seven million test hours on 1262 circuit assemblies. Circuit technologies tested include surface mount, through-hole, and hybrid assemblies. The testing consists of time at elevated temperature, as well as thermal cycles distributed over the duration of the test. Some tests also include periodic high frequency shock and vibration. All circuits are tested to failure. The tests have become more severe over time in order to better expose weaknesses as these have been discovered. Recent test results have shown a significant increase in expected lifetimes for hybrid assemblies, while surface mount lifetimes have declined. The reasons for these changes are discussed.

1. Introduction

Quartzdyne manufactures precision quartz pressure transducers sold primarily to the upstream oil and gas service industry. In order to assure the quality of the product that we sell, we have established a test procedure for all of our production circuits. The test results are used to qualify circuit assembly lots, and to provide valuable input in order to improve our process. Over time, the test results have allowed us to compare different processes, vendors, and circuit technologies, and to identify and address the weak links. The test results also provide a baseline from which field life can be predicted. Results of these tests have been presented earlier [1], [2]. The focus of this update is on observations over the last 2 years.

2. Test Circuit

The test circuit consists of three oscillators, two mixers, CMOS output drivers, and a regulator. Active components include discrete transistors, small transistor arrays, CMOS inverters, and a voltage reference. The circuit is dominated by passive components, including approximately 25 resistors and 30 ceramic capacitors. Figure 1 is a photograph of circuits typical of those tested. A digital version of the circuit is also included in the tests. The digital circuit includes a field programmable gate array (FPGA) which implements a frequency counter and a communications protocol.

The same circuit has been built using four different technologies. Low-Temperature Surface Mount (LT-SMT) uses commercially available surface mount components and processes. Plastic packaged IC's and SOT transistors are attached using SnPb solder in a convection reflow process. The High-Temperature Surface Mount circuit (HT-SMT) is the same as the LT-SMT except that components are attached with either CASTIN® [3] or Innovalloy® [4] solder. The Thru-Hole circuit uses custom components rated at or above 200°C and attached using HMP solder. This technology is no longer supplied by Quartzdyne, and discussion of it within this report will be minimal. The Hybrid circuit uses an alumina substrate with doped Au conductors [5]. Components and die are attached using a combination of conductive and non-conductive polyimides and eutectic solders. Both Au and Al wire bonds are used based on the die metallization [6]. The substrate is packaged in a custom seam-welded metal package. External wiring is direct to the Hybrid package.

3. Test Procedure

A percentage of every lot of circuits built by or for us is destructively tested. The test (Life/Cycle) includes a mixture of time at temperature and thermal cycling. Some units are also subject to high frequency vibration or shock testing. To simplify testing, units are not powered during the test. This is justified by the very low power consumption of the circuit under normal operation (<50mW), and has been validated by testing a smaller number of circuits in continuously powered tests.

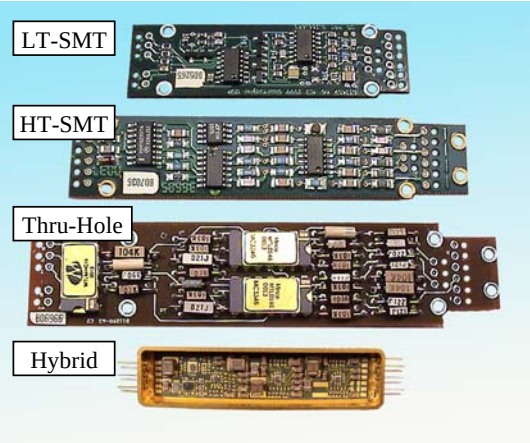

Figure 1. Oscillator Circuits Tested

Time at temperature and thermal cycling are accomplished using forced-air ovens running continuously at the maximum test temperature for each technology. Samples are left in the ovens over night and on weekends. Each working day, the samples are removed from the ovens and allowed to cool to room temperature for approximately 30 minutes, after which they are returned to the ovens for a minimum of one hour. The process is repeated such that each sample receives 15 thermal cycles and 160 hours of time at temperature each week. The units are tested electrically at ambient temperature every two to six weeks

Surface mount units are also subjected to ultrasonic vibration to expose weakening solder joints. For the hybrid units, a portion of the test sample is subjected to high-impact shock testing. The test is a 10 inch free-fall with a metal-to-metal impact, repeated 25 times. The impact is not instrumented, as we have not found an accelerometer capable of surviving this test. We estimate the impact to be approximately 1 million g's in 1 microsecond based on extrapolation of data measured at lower impacts. This sequence is repeated biweekly until 100 drops have accumulated. The Thru-Hole boards are not subject to shock or vibration testing. We know that the Thru-Hole design is not mechanically robust, and have never recommended it for high-shock applications.

We have found that the combination of tests described is much more effective than the same tests performed separately. Our first attempts at independent ageing, thermal cycling, and shock and vibration testing did not expose faults that were obvious when boards were subject to normal use. Each portion of the test suite is the result of identifying a particular failure (either in the field, or during processing), and then searching for a test that exposes that failure mode. Consequently, the tests have become more severe over time.

Since 1998, over 7 million test-hours have been logged on 1262 circuits. For each circuit there is a primary temperature where most of the data has been taken (highlighted entries in table Table 1). Several small-scale tests have also been performed at off-temperature points, but these do not have the statistical significance of the larger tests.

Table 1. Life/Cycle Test Matrix: Primary Tests are Highlighted

Test ID	Qty	Test Hours	MTTF
DL-SMT (150°C)	31	107,241	3,701
LT-SMT (150°C)	202	1,949,732	5,204
LT-SMT (180°C)	2	3,600	1,800
HT-SMT (150°C)	2	38,100	19,050
HT-SMT (180°C)	475	831,266	552
HT-SMT (200°C)	2	1,392	696
Thru-Hole (150°C)	1	23,304	23,304
Thru-Hole (180°C)	1	6,648	6,648
Thru-Hole (200°C)	119	464,438	4,033
Thru-Hole (225°C)	2	1,520	760
Hybrid (225°C)	397	3,855,038	10,566
Hybrid (250°C)	28	47,237	4,033
Total	**1,262**	**7,329,516**	

4. Test Results – Surface Mount

Plotting the survival rate of the primary tests versus test time at each observed failure yields the plot in Figure 2. Each point is calculated as the number of units that have survived at least that long divided by that total plus all prior failures. The smoothed lines on the graph are a best-fit Weibull survival model [7], [8]. From the smoothed lines we can predict time-to-failure based on all of the data points in the test. Figure 3 is essentially the same plot as Figure 2, except that the data set is limited to parts manufactured in the last two years. The survival rate based on 6 years of data is also plotted in Figure 3 as dashed lines for reference.

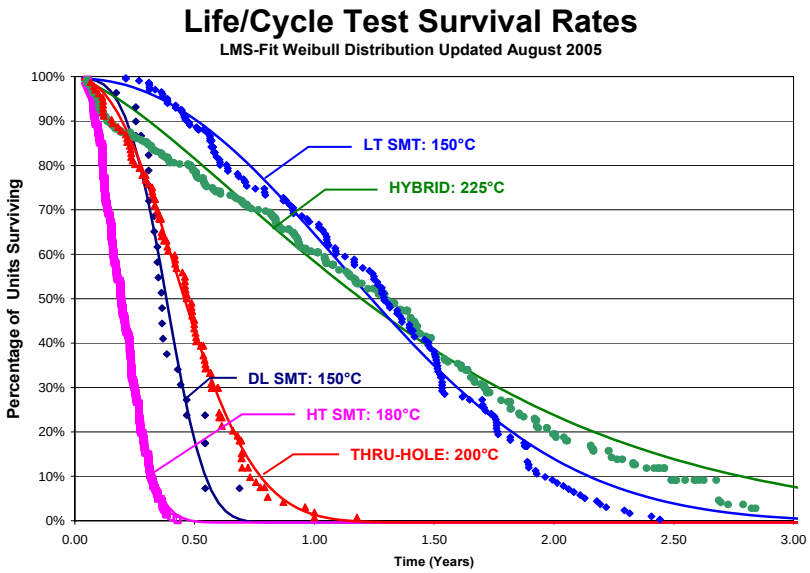

Figure 2. Survival Rate plotted at each failure time for primary test temperatures. Smooth lines are best-fit Weibull Survival Function based on testing from April 1998 through July 2005.

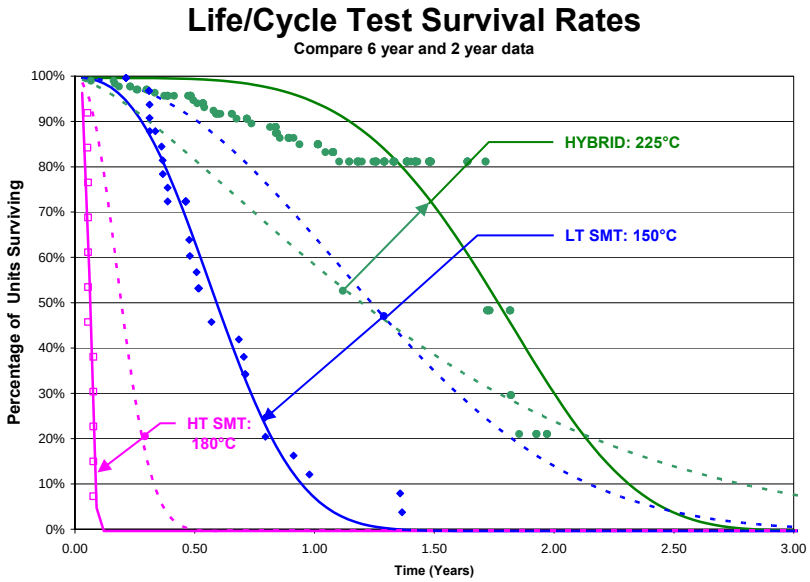

Figure 3. Survival Rate plotted at each failure time for the last 2 years only (July 2003 through July 2005). Solid lines are best-fit Weibull survival function for 2 year data. Dashed lines are from 6 year data. Note the improvement in Hybrids, while the SMT technologies have become worse.

The projections are clearly different for the recent data, indicating a significant process change. The lifetime for both of the surface mount technologies has dropped in half. This can be explained by recent industry trends towards using plastic IC encapsulants with higher Bromine content. Bromine halogens are commonly used as a flame retardant.

At high temperatures these break down and accelerate corrosion of the Au-Al wire bond. The higher Bromine content, coupled with other related resin changes has been shown to decrease the life of the wire bonds at temperatures above 125°C [9],

The European Directive on Hazardous Substances in Electrical and Electronic Equipment (RoHS) has called for a ban on certain brominated flame-retardants by 2006. Electronics manufactures are responding by developing bromine-free encapsulants, and these are starting to become commercially available. Results of tests of a bromine free FPGA package are very promising. Where the brominated FPGA packages routinely failed at 3000 hours, we now have two units which have survived over 6600 hours using this package, and an additional 5 units are at 4500 hours with no FPGA failures. We are working towards switching all of our SMT plastic components to the newer package type, but several vendors have been slow to respond.

5. Hybrid Failure Analysis

While the Hybrid test results demonstrate a clear advantage over the other technologies, Figure 2 also shows a high number of early failures and a broad distribution of failure times for those Hybrids. This is indicative of a process that is not in complete control. A tighter process would yield a survival function that stayed high initially, and then dropped off steeply as the wear-out mechanism began to dominate. As can be seen in Figure 3, the units built in the last 2 years are significantly better than earlier units, showing a much higher early survival rate. An analysis of the failure modes and process changes over the past several years will help to explain the change.

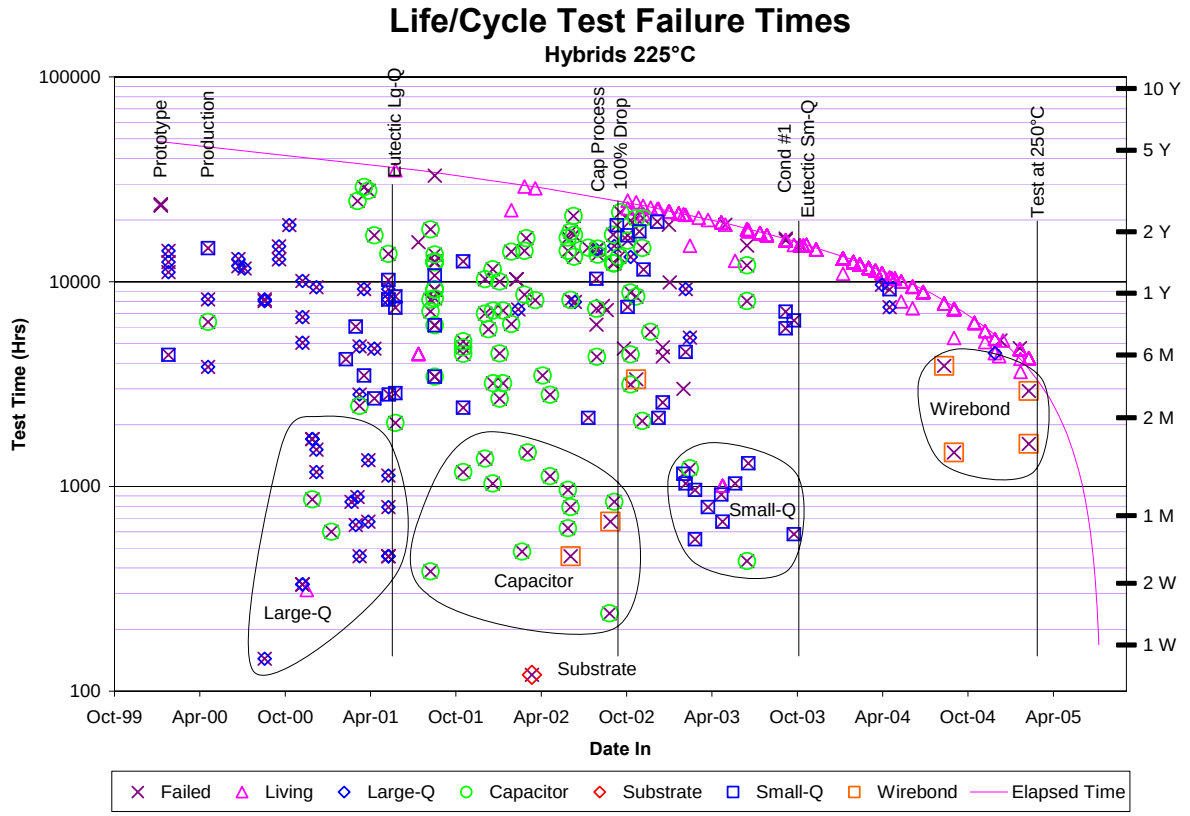

Figure 4. Test times for production hybrid units in Life/Cycle test at 225°C. Failed units are denoted with an "X"; open triangles "Δ" indicate units still surviving. The latter generally follow the elapsed time line until failure. Failure modes and key process changes are also identified.

In Figure 4 the test time for each hybrid unit is plotted versus the date the unit was initially put into test. Units which have failed are marked with an "**X**"; units still surviving, with an open triangle (**Δ**). Key process changes are identified along the top of the graph. Failure modes are indicated by various symbols and labels as shown in the key. As can be seen, there areobvious groupings of early failure modes which correlate with the process changes.

The first four prototypes survived nearly 24,000 hours with a very tight distribution. (They appear as a single bold "**X**".) The first batch of production units showed a much broader distribution with an average of 8200 hours. In our experience, it is not uncommon for initial prototypes to behave better than production units given the care and attention paid to these units.

The first significant problem to appear was a high-impedance collector-to-substrate connection on a large transistor used in the regulator (Large-Q). As this problem became more prevelant, a solution was identified. In May of 2001, the conductive polyimide used to attach these components was replaced with a eutectic solder. This solution completely eliminated infantile failures of this class. The few failures of this class shown in 2002 and 2003 are related to the eutectic attachment and occurred at approximately 8,000 hours.

The next significant failure mode was breakdown of the conductive polyimide used to attach capacitors (Capacitor). This failure mode was highly random; one particular lot had an initial failure at 384 hours, while the other units in the same lot lasted 7,000 and 18,000 hours respectively. The problem appeared to be related to process variation rather than a fundamental limit of the materials. Several attempts were made to address the issue which was finally resolved with a series of process changes implemented in August 2002.

Two additional problems are indicated in the graphs during this time frame: a poorly attached substrate (Substrate) and some marginal wirebonds (Wirebond). While Life/Cycle test failures for substrate attachment were rare, field failures for this mode were disturbingly high. A 100% high-impact drop screen was implemented in September 2002 which effectively screened for both of these problems. This screen is also effective at exposing capacitor attachment problems. By screening 100% of all units we not only increase our confidence, but are able to provide timely feedback to the vendor, allowing faster response to problems. The substrate attach problem was completely solved by a process change, and we presently see very few failures of any kind in the initial screen.

A failure mode involving a pair of small transistors began to dominate in April 2003 (Small-Q). As shown, the failure mode existed as early as April 2000 above 3000 hours. Only after the other problems had been reduced did it reveal itself as a dominant failure mode. In fact, it is the same failure mode that the larger transistors showed, but the circuit is less sensitive to it in the smaller transistors. The same eutectic attachment solution used earlier on the larger transistors has been similarly effective on the smaller ones.

Since October 2003, wirebonds have become the dominant (and only) early failure mode. The drop test implemented in 2002 went a long way to eliminate this problem, but it appears to be creeping back in. We are presently pursuing ways to improve both the quality and consistency of the wirebonds.

At the time of this writing, there were more than 175 Hybrid units surviving in the 225°C test. With typical test durations in the 1-2 year range, this test has become onerous, and we have decided to increase the test temperature to 250°C for new units going into test. It is hoped that this will give more timely feedback on process weaknesses as well as reducing the workload associated with testing so many units for so long. To date, 28 hybrids have been put into the 250° test (Table 1). Test failure modes have been consistent with failure modes noted in the 225°C test.

6. Predicting Field Life

Thus far, we have only considered the data at the primary test temperature for each technology. Several small scale tests have been performed at alternate temperatures, and while these may not be statistically significant, they do suggest a reasonable de-rating factor. In Figure 5, the time to failure for each of the test points has been plotted versus the test temperature. The time to 50% failure is plotted along with error bars at the 10% and 90% failure times as derived from the Weibull fits described earlier. In addition, the commonly used 2x/10°C de-rating curve has been plotted to give an indication of a possible de-rating.

It can be seen that the 2x/10°C de-rating is a reasonable approximation for most of the technologies. The exception to this rule is the Hybrid plot where the 250°C data is a little higher than would be predicted from just the 225°C data. This can be explained by the process changes discussed earlier. When plotted with data from just the last 2 years (Figure 6), the Hybrid data points line up much better, as do the various SMT lines. The Thru-Hole data has been eliminated from Figure 6, since no Thru-Hole circuits have been put into test in the last 2 years.

The HT-SMT and LT-SMT projections are quite close to each other. This is consistent with the package related failure mechanism discussed earlier, which is independent of the solder process [9], [10]. The separation of the DL-SMT from the HT-SMT and LT-SMT projections is misleading in the 6-year data as the latter projections are dominated by the earlier tests. As plastic package composition has changed, the life of all of the surface mount technologies has decreased uniformly.

The ultimate goal of Life/Cycle testing is to provide quality product, along with the information required in order to use that product with confidence. The data presented here is only a starting point towards that end. Actual field life is dependent on the specific environmental stresses to which the product will be subjected. The Life/Cycle tests were originally designed to push the limits of stresses that may be encountered in logging and drilling environments (elevated temperature, rapid thermal cycling and high mechanical shock). Because of the severity of these tests, we would expect field life in a *typical* application to be greater than or equal to the lifetimes predicted by this test data. A full discussion of field reliability of Quartzdyne Transducers is covered in a separate report [11].

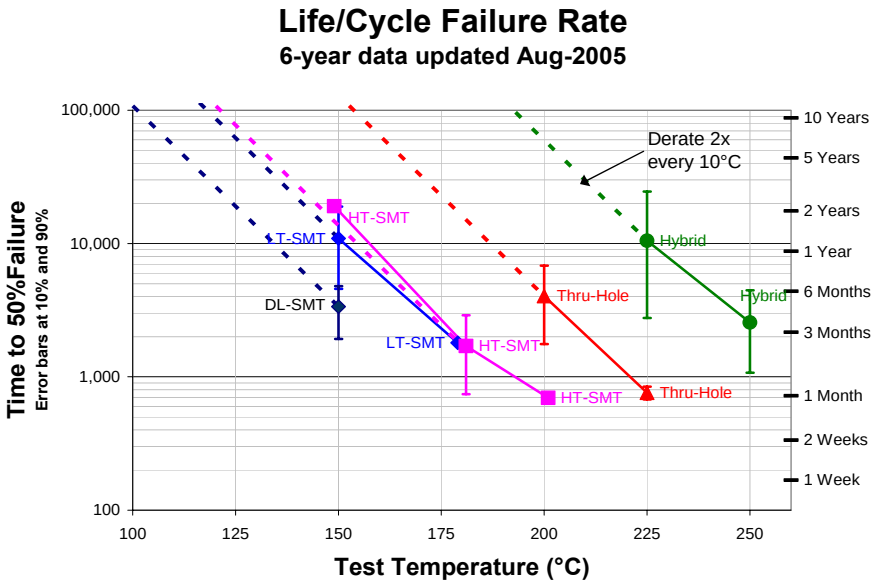

Figure 5. Life/Cycle test time to failure based on 6 years of testing.

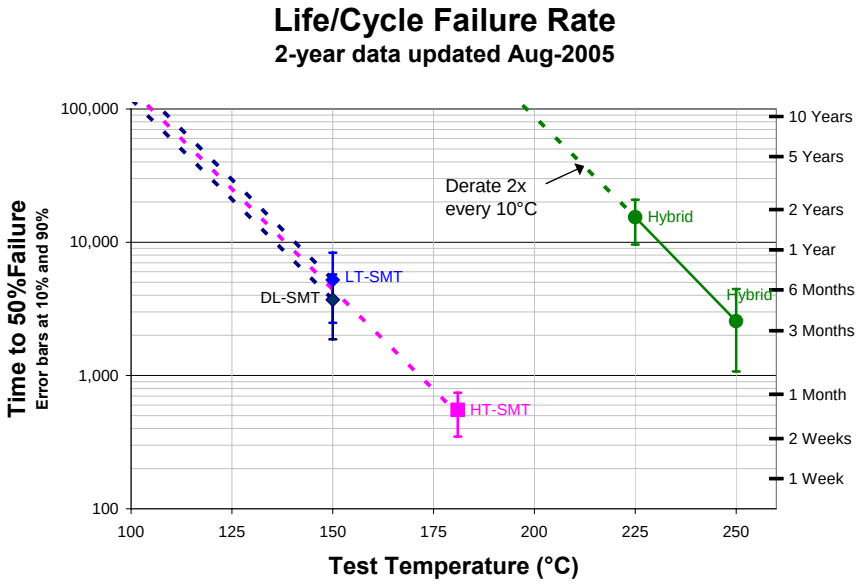

Figure 6. Life/Cycle test time to failure based on last 2 years of testing.

7. Conclusions

A simple declaration of a maximum operating temperature is not adequate when specifying a product for use in a down-hole environment. Time at temperature, thermal cycling, and shock and vibration are all critical factors in determining circuit life in this hostile environment. Subtle process changes, whether intentional or not can also affect circuit life. Systematic destructive testing is a valuable tool that can be used to monitor quality and to predict useful life of the product.

Surface mount Sn63 with commercially available components and packaging can be used for applications not exceeding 150°C. Lifetimes of 1 year at temperatures below 125°C can be expected with present plastic packaging in typical down-hole applications. A switch to better plastics is needed to improve these lifetimes to historic levels. Since the limiting factor at these temperatures is package related, rather than solder related, simply switching to exotic solders will not improve the service life.

For temperatures above 150°C, custom packaging is required to achieve lifetimes beyond a few months at temperature. For short excursions up to 200°C, through-hole components can be utilized with appropriately selected

components. For extended time at temperatures above 125°C, carefully constructed hybrid circuit assemblies are preferred. Careful monitoring, and continuous process improvement has yielded a technology and process that can be used for several years at temperatures up to 200°C, with short-term excursions as high as 250°C.

8. Acknowledgements

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9. References

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