Characterization and Reliability of custom digital ASIC designs using a 0.8µm bulk CMOS process for high temperature applications

Mark Watts, Shane Rose
Quartzdyne, Inc.
4334 W Links Drive
Salt Lake City, UT, 84120
801-839-1000, markwatts@quartzdyne.com

Abstract

With today's quickly changing technology, part obsolescence often forces unanticipated and costly design changes outside the normal product life cycle. Custom ASICs can be used to fill this gap and gain other advantages such as reduced parts count, higher performance, and higher reliability. Two digital 0.8µm bulk CMOS ASICs have been successfully implemented, providing higher reliability and performance than their replacement parts at 225°C. In this paper we examine some of the design issues encountered during their implementation, including process selection, library characterization at 225°C and above, performance, testing and qualification. External analog circuitry was integrated to further reduce parts count and increase reliability. In conclusion, we have found bulk CMOS to be an acceptable process for custom ASICs in high temperature environments.

Keywords: High Temperature Electronics, Bulk CMOS, Reliability, Digital ASIC

Introduction

Development of custom ASICs is considered a solution to replace high cost FPGAs and ward off costly design changes as standard parts are increasingly phased out or discontinued. Other advantages are increased reliability, increased performance, and a smaller footprint. Recently two digital ASICs have been developed that have been successful in meeting these objectives.

Obsolescence

The first ASIC (ASIC-1) was designed to replace an FPGA with the expectation that the performance would be better and the return on investment would be beneficial. ASIC-1 has been used in production since July 2009. The development cost has been recouped and the part performs better than the one it replaced. This alone has been a big win. Later, a minor modification of ASIC-1 allowed us to move forward when a memory part in the circuit was discontinued. The old memory had poor yield and was not very reliable. It ran on 2.5V, while other memories being considered required 5.0V. In anticipation of upgrading the memory, a pin option was added to select between 2.5V and 5.0V IO to the memory. A new hybrid substrate was also under development to handle the new parts. Prior to making the normal product transition, the memory vendor informed us that they were discontinuing the memory. The parts we had in stock would only last for a few months. Fortunately the new substrate and the ASIC modification were ready to go. After a relatively smooth transition the upgraded product works better and is more reliable.

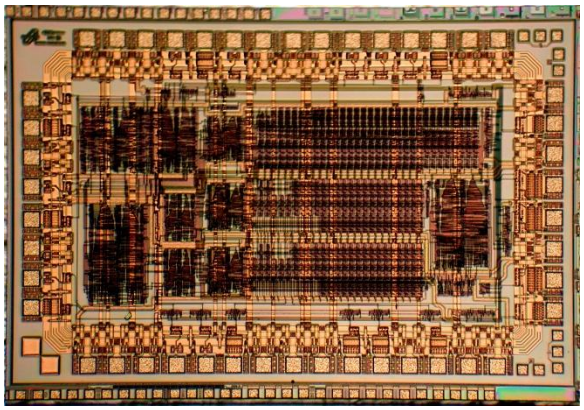

Figure 1. ASIC-1

The second ASIC (ASIC-2) was also designed to replace an FPGA and integrate a few analog parts with the same goals as stated previously. The hybrid using ASIC-2 replaces a hybrid that had problems in high vibration environments. A decrease in die size and elimination of other parts is expected to make the new hybrid less susceptible to vibration, easier to build, and more reliable. ASIC-2 was fabricated in February of 2012. The analog and digital functions have been tested in the lab and found to be within specification. The product is scheduled for testing and qualification in the second quarter of 2012.

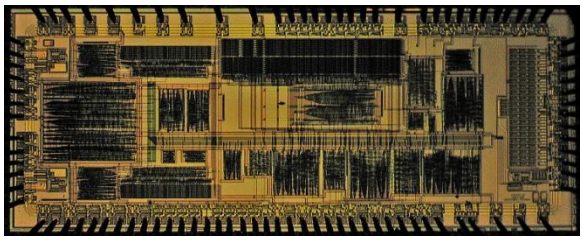

Figure 2. ASIC-2

Process Selection

The first step in selecting a process is to define the design constraints. Both ASICs operate on 2.5V-5.0V over a temperature range of -40 to 225°C. Low volumes of 500 to 2000 pieces per year are expected. ASIC-2 requires a 50V IO driver. The ASICs are purchased as bare die because the die will be attached directly to a hybrid substrate.

Table 1. Process Selection

Process		
Constraints	**Failure modes**	**Tools**
2.5V – 5.0V	Latch-up	Logic sim
-40°C - 225°C	Metal Migration	Spice
Bare die	Hot carriers	Synthesis
500-2000 pieces	Gate dielectric breakdown	Extract
50 V devices		DRC, LVS
		Layout
		Chip assembly

Second, process limitations and failure mechanisms are considered. The issues are latch-up, metal migration, hot carrier effects, and gate dielectric breakdown. Design techniques can be used to minimize the adverse effects of most of these physical limits as discussed in [1].

Third, low-cost design tools are desired and a standard cell digital library is needed. Design tools required for digital design are a logic simulator, synthesizer, place & route, chip assembly, layout, net list extraction, and Spice simulation. Past experience with the XFAB has proven that their bulk CMOS 0.8µm process meets all of the above requirements. Of particular note is 2.5V core operation for both digital and analog functions, low volume support, low-cost design tools support, and a low-power/low-voltage standard cell library. XFAB has a process option for 60V structures in their CMOS 0.8µm process so the decision was made to continue using this process.

Test Chip

A test chip was designed to make sure the digital library works at 2.5V, determine operating temperature range, measure leakage current, and generally show that the process works for the intended product. Structures were included for measuring leakage and gate delay. The test chip was designed with IO in the same locations as ASIC-1 so that the ASIC-1 probe card could be used. A hot chuck and LabVIEW station were used to perform the tests.

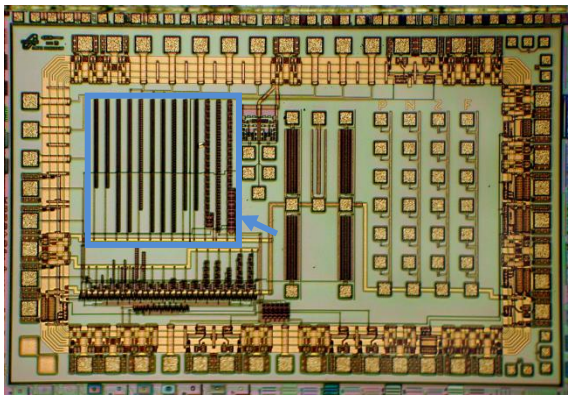

Figure 3. Test Chip

The leakage for arrays of eleven gate types (highlighted in Figure 3) is shown in Figure 4. The data, which is not normalized, reflects the leakage of each array of gates. The trend shows that the logic gates should work up to 250°C before leakage starts to become a factor.

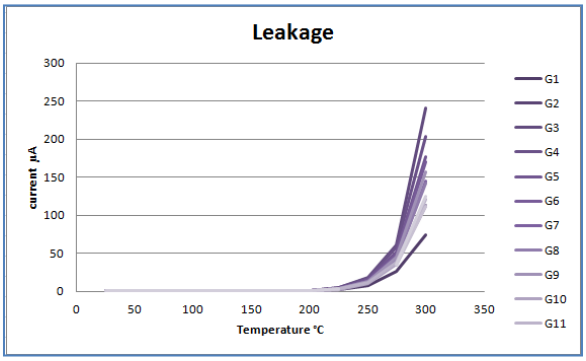

Figure 4. Leakage data from test chip

Adding Features

A complete and comprehensive specification is essential to expedite the design in a timely manner. The specification includes a description of the part, special features, block diagrams, schematics, flow charts, IO specifications, and test descriptions. In addition to this collection of documents, HDL code

and test patterns serve as a "golden" simulation standard. A working prototype with an FPGA sourced by the HDL code assures a higher probability of success.

Table 2. Specification requirements

Specification	
Documents	**Code**
Description Features Block diagrams Schematics IO Specifications Test descriptions	HDL code Test patterns

Implementing a straight conversion of an FPGA to a custom ASIC has significant advantages. In particular, the die size is smaller and less expensive. The ASIC will consume less current, work at higher temperatures, and generally will have better performance.

At this point, however, the specification effort is not complete as enhancements to the system have yet to be considered. They can include integration of external parts, adding features, layout optimization, compatibility, and testability.

Adding features has its risks and benefits. Some features are a definite win, while others may be compelling but not get used. Sometimes customers say they want a feature, but a different solution may actually satisfy their requirement better. Backward compatibility must also be factored into the design. Some features may be outdated or seldom used, and eliminating them can save area and design effort. New features require careful evaluation and must be clearly documented in the specification at the beginning stages of the design. The testing of new features must also be added to the test specification and pattern set. Table 3 shows the main feature changes for ASIC-1 and ASIC-2.

Table 3 . Added features

	ASIC-1	ASIC-2
Features	1. startup time 8ms/32ms 2. dual mode T/P pins 3. analog/digital mode 4. parity check 5. clk_out 1KHz/7MHz 6. JTAG 7. dual voltage memory	1. remove barrel shifter 2. reduce four I2C modules to two 3. fast test mode 4. power off external part (2x) 5. high voltage switch (2x)
Integration	1. I2C on chip	1. I2C on chip 2. voltage regulator (2x) 3. 8:1 analog mux 4. 50V IO driver
Optimized	1. serial divider 2. dual counters (2x)	1. distributed memory bus 2. I2C interface (2x) 3. instruction decode

Layout optimization consists of finding certain well-defined structures that can be tiled for a significant size and performance advantage. For example, a multiplier can be implemented more efficiently as a tiled array rather than a standard-cell module. Implementing layout optimization for a module also includes generating a matching gate level model for simulation and later layout vs. schematic (LVS). Layout optimizations require more design effort but the payback is usually high. These optimizations do not change the specification or simulation results.

Backward compatibility must be maintained. Below are two examples of a product improvement that had compatibility issues when we thought the product was backward compatible.

1. A customer was using an undocumented feature that was discovered by trial and error. ASIC-1 was implemented to conform more closely to an industry standard specification but the customer's use of the hidden feature caused the system to fail with the new part.

2. ASIC-1 operates with less current than its predecessor. One customer's incoming inspection procedure failed because the current was too low. The customer ultimately modified the inspection limits.

Testability affects simulation time for design iterations, debug of first article parts, and the ability to determine if the part works prior to deployment. Different approaches to testability were used in the ASICs we are examining.

ASIC-1: A JTAG scan path was implemented, making it possible to test counter conditions that otherwise could not have been set up in a time-efficient manner.

ASIC-2: A "fast" mode pin was implemented that allows the chip to be simulated and tested in 500ms instead of 120sec. The 500ms simulation takes approximately one hour of simulation time while the 120sec simulation takes approximately 40 hours. Using the fast mode was essential for development and debug of the design. It also reduced the pattern set for wafer probe to a manageable size.

Production testers used for wafer-test have limits and the one our vendor is using has a limit of 16M patterns. At 4 samples per cycle the 500ms simulation is 14.6M vectors. In table form the pattern file was too big to compress. Using the value change dump (VCD) format the patterns were 338MB. This file was compressed into 53MB and sent via FTP to the test vendor. There is no way the part could be tested using the 120sec pattern set. (Note: This is real time for wafer-test).

Adding test structures or test modes increases real estate and usually requires additional pins. This must be added to the specification.

Finally, the complete specification covers the original device specification, detail for external parts to be integrated, added features, layout optimizations, compatibility, testability strategy, and additional tests. All of these enhancements contribute to the performance and reliability of the new system.

Simulation

Simulation is the process used to verify that the design works as intended. The digital logic is verified with a logic simulator and analog modules are verified with Spice simulation. Clock skew, critical paths, and asynchronous circuits are verified with Spice.

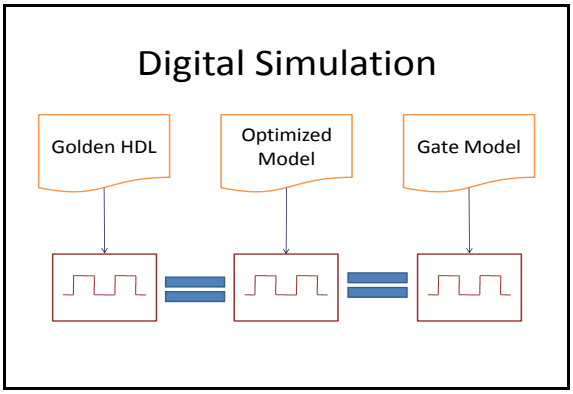

Figure 5. Three simulation models. Simulation outputs must match.

During logic simulation, digital stimulus is applied to a model of the design, the simulator calculates what happens and the outputs are observed. In our ASIC designs there are three models: the golden model, the optimized model, and the gate-level model. The golden model is the proven design and is, in a sense, the specification. The optimized model matches the layout optimizations and includes any added features. The gate-level model has a one-to-one correlation to each layout gate and has back-annotated delays based on extracted capacitances. The same stimulus is applied to all three models and the response is expected to be the same.

Performance is assured in logic simulations by derating the simulations. For ASIC-1 the simulations were run at 4.3x the expected application frequency [2]. This provides margin for voltage, temperature, and process variations. A second check is the timing report from the synthesizer. Each module must meet the derated frequency goal. Figure 6 shows an example simulation waveform.

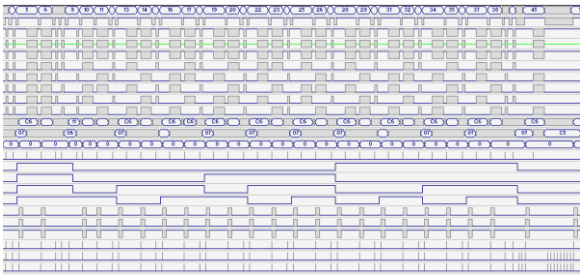

Figure 6. Simulation waveform.

Asynchronous modules are treated separately. They are designed and debugged using Spice simulations. Simulating asynchronous signals in digital simulations often causes the whole design to go unknown erroneously, so cross-domain clocks are set to be the same or tightly related. This also simplifies wafer test where tester limitations make it difficult to fully test asynchronous circuits.

Analog cells are verified via Spice over the process corners, voltage limits, and temperature range. Simplified simulation models are written for the logic simulator. There are currently efforts by simulation vendors to do mixed mode simulations running Spice and digital simulations at the same time [5]. Clock tree skew and critical paths are also simulated with Spice. Figure 7 is a Spice simulation of clock skew. The traces marked with ellipses are the last stage of the clock buffers.

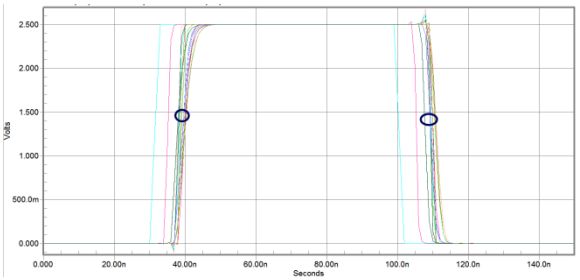

Figure 7. Spice simulation of clock tree skew.

After layout, the layout net list is extracted and compared to the synthesized net list using the LVS tool. When this passes, the gate level net list is generated and annotated with realistic delays. This gate level model is simulated and the outputs are compared to the golden simulation.

Layout

There are two main phases to layout. Floor planning is done at the start of the design to estimate a realistic chip size and make pin assignments. Later,

after new features are added and the layout model is verified, real layout begins.

During the floor planning stage modules are quickly synthesized, then place & routed to get relative size and signal relationships. Modules are selected for optimization. Pin assignment is coordinated with the substrate design effort and the internal chip module placement as well as internal signal routing. Power pins are distributed generously and especially near output pins to reduce ground bounce.

After the optimized model is verified via logic simulation, layout begins. Clock and power routing widths are determined in order to meet skew and metal migration constraints. Power bus widths are used in the auto-router as synthesized modules and implemented using standard cell place & route tools. A clock strategy is determined for minimizing skew between registers. The clock tree is designed to have the same number of logic levels from the primary clock to each of the individual registers.

With the power framework and clock strategy determined individual modules are laid out. Optimized modules are tiled by hand. Modules are carefully placed to minimize routing and then interconnected with chip assembly and layout tools.

Extra gates are added to allow for metal fixes at a process hold in case things are not right the first time. This has proven to be extremely valuable in both designs.

For ASIC-1, an inverted output pin was corrected, a math error in some high order bits fixed, and a pin option feature was changed using the metal-hold option.

For ASIC-2, a counter was extended by two bits, a memory bus conflict and some incorrect logic were fixed.

There are various reasons for these errors: insufficient coverage of test patterns; mismatch between analog and corresponding simulation model; and changes in the specification or feature set that are not propagated to all affected areas.

As experience is gained, improvement is made in the extra gates cell. For example, in ASIC-2 more inverters were added and used.

Verification

Layout spacing rules are verified via Design Rule Check (DRC) in the layout tool. The layout tool is used to extract a transistor net list from the layout. It also extracts loading capacitance on signals later used for back annotation. A transistor level version of the schematic is derived from the synthesized gates and optimized cells. Each gate has a transistor implementation that matches the layout. LVS is used to compare the layout net list to the schematic net list and build a net equivalence file between the layout and schematic. When the two net lists are identical an Standard Delay Format (SDF) annotation file is generated that specifies the delay for each gate based on the extracted capacitance and the net list equivalence file. The gate level model with back-annotated delays is simulated and the outputs are compared to the golden simulation. This usually brings out slow signals that need buffering as well as other timing problems. Buffers are inserted, and after a few iterations the gate level model passes.

When DRC, LVS, and the gate level model pass, the mask data is prepared for the foundry and sent to be fabricated. This significant milestone in the design is typically referred to as "tape-out." During fabrication many copies of the design are fabricated on silicon wafers.

Complete verification is the successful completion of logic simulation, analog simulation, DRC, and LVS as discussed so far.

Validation

After fabrication, some die on a wafer are tested in-house for functionality. Typically some bugs are found, and extra gates are used to fix them using the metal -hold option from the foundry. After a design is proven to work in-house, a wafer and test patterns are sent to the test vendor for testing and dicing. Bringing up the test patterns for the first time usually takes some coordinated effort with the test vendor.

Results

First-pass silicon for ASIC-1 was found to operate up to 280°C. A few bugs were found and extra gates were used to fix them. The metal fix version works fine and has been successfully used in production since 2009. For the second revision of the part, an option to interface to 5V memory as well as 3.3V memory was added. This proved to be invaluable when the memory vendor of the 3.3V memory informed us it was being discontinued.

First-pass silicon of ASIC-2 had bugs that were fixed using extra gates. It has been tested to work up to 265°C and preliminary tests of the 50V outputs show them to withstand up to 90V at 225°C before breakdown. The design has been tested at the wafer level with a 90% yield and is currently being integrated into product.

Analog functions integrated into ASIC-2 are a 50V communication driver, a current-limiting voltage regulator, and an 8-input analog multiplexor. In comparison to the FPGA it replaces, the digital

core runs with less power and the chip has a smaller footprint. Bringing the analog functions on board protects against part obsolescence for those functions. The bulk CMOS implementation performs well at 225°C with less current.

Parts Count Reduction

Production is simpler with fewer parts. The parts count for the hybrid using ASIC-1 reduced from 92 to 37 with room left over to allow optional features. For example, any of three different voltage regulators can be used. In Figure 8 the mapping of discrete components and their corresponding ASICs is highlighted.

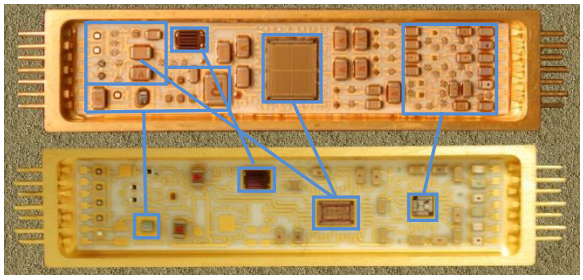

Figure 8. Top: Discrete hybrid with FPGA. Bottom: ASIC hybrid with ASIC-1.

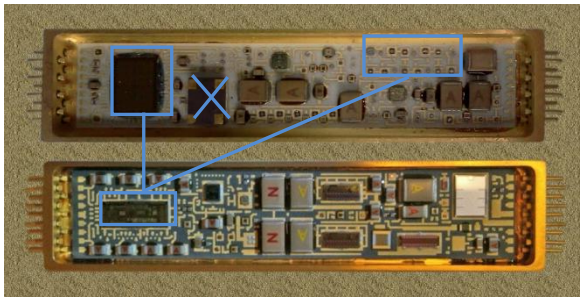

Figure 9. Top: older hybrid with FPGA. Bottom: hybrid with ASIC-2.

The parts count for the hybrid using ASIC-2 reduced from 90 to 58. The hybrid actually looks more dense. Many features were added and two discrete voltage regulators were replaced with commercial ASICs. The FPGA and seventeen discrete parts used for the 50V driver are integrated into ASIC-2 and shown highlighted in Figure 9. A fairly large oscillator "X" was eliminated and the replacement clock supplied externally by a feature added to ASIC-1 in a different part of the system. The large oscillator was problematic in high vibration environments and by removing it the system is more reliable.

Performance

Supply-current data is compared in Figure 10 for the system containing ASIC-1 and its predecessor with discrete circuits and the FPGA. The ASIC-1 system also contains two custom analog ASICS [2]. The significant current draw starting at 180°C for the discrete design is a compelling argument to use the ASIC technology for systems operating above 180°C.

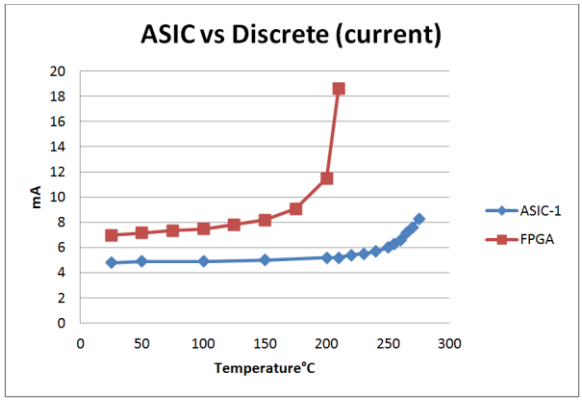

Figure 10. Supply current comparison of ASIC-1 vs. Discrete system.

The plot in Figure 11 shows the current for a system with ASIC-2. The top data labelled "xd0 xd1" is the current when the system is operating with a full load. The two middle traces show the current when one or the other load is removed. The bottom line is the current in the digital core. This plot indicates a fairly flat current consumption from ambient to 250°C.

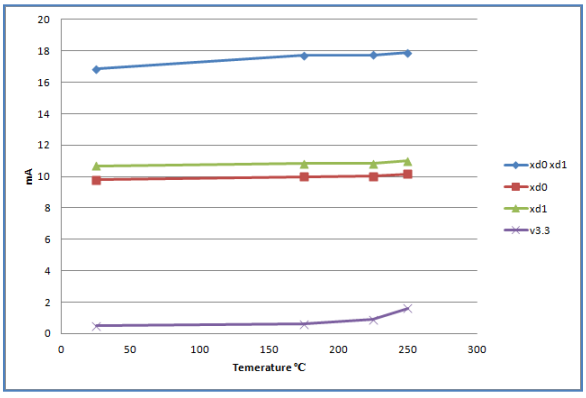

Figure 11. Supply current of ASIC-2 system over temperature.

Reliability

Tested dies are placed in inventory and a few first article units are built. These units are used for qualification through accelerated life tests and powered life tests. Periodically during production more units are sampled and added to the qualification pool. All of our units are also subjected to a drop test. Over the years we have developed die-attach and bonding technology that withstands our extreme tests.

Historical failure data has been taken for products using ASIC technology vs. discrete technology. The ASIC technology includes ASIC-1 and two other custom analog parts [2]. Using accelerated life tests, 90% of the ASIC based units lasted nine months while the 90% of the discrete units lasted only 6 weeks as shown in Figure 12. In other words, the ASIC based system is significantly more reliable [3, 4] and we expect that the system with ASIC-2 will have similar success.

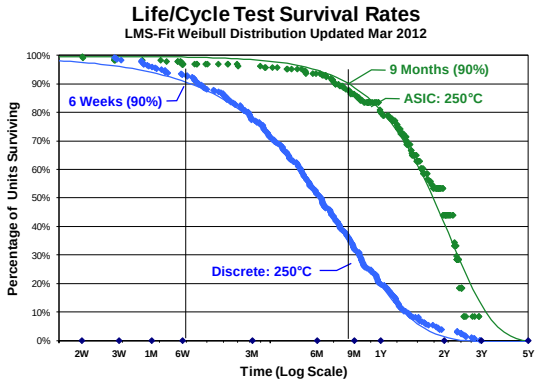

Figure 12. Hybrid with ASIC-1 vs. its predecessor survival rate.

The life/cycle data in Figure 13 shows hybrid-based products to have a significant advantage over SMT-based products at higher temperatures. It also shows ASIC based products to have an advantage over discrete based products. The solid tail for ASIC hybrids is more recent data than previously reported [3, 4].

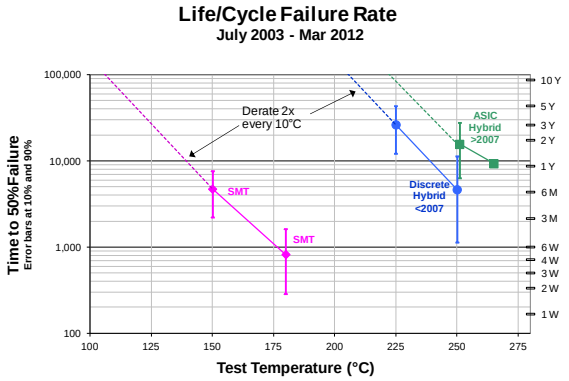

Figure 13. SMT, Discrete, and ASIC Hybrid failure rate comparison.

Evaluation

The relative complexity of the ASIC designs is indicated in the table below by the number of gates and features added. The added features, integration of external components, and layout optimizations all factor together to increase the producibility and reliability of the hybrids into which they are integrated.

Table 4. Relative design complexity of the two digital ASIC's. Number of features added, external components integrated, and layout optimizations.

	Gates	Feat	Ext	Opt
ASIC-1	5,586	7	1	2
ASIC-2	22,087	5	4	3

ASIC-1 has had two revisions to date (see the Table below). Note that the current increased in Rev1. This is due to adding a clock output feature of 7.2 MHz. This feature was used in the ASIC-2 hybrid to eliminate the large oscillator, thereby making it more reliable in high vibration environments. In Rev2, current reduction optimizations were implemented, bringing the current below the original pre-ASIC-1 current. Rev2 also the added a dual voltage IO option for external memory, allowing us to transition smoothly when the memory part was discontinued. The current values in this table were taken at ambient temperature. Higher temperature currents are larger but show the same trend. The table below highlights the relative reduction in parts count, die size, and current consumption.

Table 5. ASIC-1 Reductions.

ASIC-1	Parts count	Die Size	ICC Rev1	ICC Rev2
Before	92	62,640	7.4	8.3
After	37	16,430	8.3	5.5
%	40	26	112	66

A lot of features were added to the ASIC-2 hybrid (see table below). Many discrete components were eliminated as their functions were integrated into ASIC-2 and the off-the-shelf voltage regulators. The table below highlights the relative reduction in parts count, die size, and current consumption.

Table 6. ASIC-2 Reductions.

ASIC-2	Parts count	Die Size	ICC
Before	90	62,640	24
After	58	55,125	18
%	64	88	75

Conclusion

The 0.8µm bulk CMOS process has been successfully used for both analog and digital parts. ASIC-1 has been qualified and is working in production. ASIC-2 has been shown to work and the product qualification process is starting. It is expected to go into production third quarter 2012.

In conclusion, features have been added and layout optimizations implemented into two digital ASICs replacing less-optimal FPGAs and many discrete parts. In addition, analog ASICs have replaced functions previously implemented with discrete parts. The resulting hybrid designs are more efficient, have increased functionality, and are more reliable. By integrating many external circuit functions the parts count has significantly decreased, making the designs easier to produce and less dependent on vendor -supplied parts that could be or already have become obsolete.

References

[1] Shane Rose “A 225°C Rated ASIC for Quartz Based Down hole Transducers”, www.quartzdyne.com

[2] Shane Rose, Mark Watts, “Quartzdyne ASIC Developments,” High Temperature Electronics Conference, Oxford, England, 2009.

[3] Milton Watts, Ron Smith “285°C Resistor Drift and Failure Analysis”, Proceedings if the International Conference on High Temperature Electronics Network (HiTEN), Oxford, United Kingdom, 2011

[4] Milton Watts, "High Temperature Circuit Reliability Testing", Proceedings of the International Conference on High Temperature Electronics, Paris, France, 2005.

[5] Jeff Miller, Jerry Kaczynski "Bridging Analog and Digital Verification”, Aldec/Tanner EDA webinar, March 2012.