Quartzdyne ASIC Developments

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Abstract

Quartzdyne Pressure Transducers incorporate circuits that require reliable operation at high temperature, low voltage and low power. Die cost and availability are major impediments to designing high temperature electronics. High-precision, quartz-based transducers include reliable oscillator circuitry, a stable voltage regulator, and a frequency counter. These constraints are overcome by designing custom ASIC's utilizing a commercially available 0.8µm bulk silicon CMOS process. Two new 225°C rated ASIC's were developed: a voltage regulator and a frequency counter.

The voltage regulator was designed in response to the obsolescence of a commercial voltage reference die. The voltage regulator is based on a standard CMOS band gap topology, utilizing high temperature design techniques. The low dropout 2.5V regulator includes a microprocessor reset for use in digital systems. It has been shown to function above 250°C, while demonstrating more than 8000 hrs of powered life functionality at 225°C.

The Frequency Counter was designed to replace an expensive, high current drawing FPGA, while adding new features. The I²C compatible device counts the two low frequency signals and reports the ratio of signal to the reference clock. Hybrids based on this chip have 2.3x less current draw than the prior generation at 225°C, while showing functionality at 275°C. Both ASIC designs are a part of a long term plan to increase transducer functionality, remove unreliable parts, and decrease hybrid costs.

Key words: High Temperature Electronics, Voltage Regulator, ASIC, Hybrid, CMOS

Introduction

Quartzdyne pressure transducers are deployed in three main markets, Permanent, Logging, and Drilling. The permanent market requires long term reliability, because the transducers are typically irretrievable. The battery-powered logging and drilling markets require low voltage operation, and are very sensitive to current draw. Most well temperatures are less than 200°C, with only a small percentage of wells reaching 225°C or higher.

High-precision, quartz-based transducers require 3 circuits: a reliable oscillator, stable voltage regulator and a frequency counter. Prior generations of Quartzdyne transducer electronics are based on discrete die components and a FPGA. The fading availability and cost of these components with their resulting circuit functionality restrictions has pushed Quartzdyne electronics designers to use custom ASIC's.

ASIC designs are completed using a commercially available bulk silicon CMOS process to meet the low voltage, low current, and high temperature requirements. XFAB's support of low cost CAD tools, Multi Layer Mask (MLM) & Multi Project Wafer (MPW) runs, 6 wafer engineering runs, and their overall lower cost made them a good choice. Designs are fabricated in a 3 metal 0.8µm configurable process. Process options include three polysilicon resistors, a poly1-2 capacitor, a few BTJ transistors, and higher voltage MOSFETs.

High temperature bulk silicon design techniques and failure mechanisms have been studied in the past [1,2,3]. The design techniques focus on preventing latch up and understanding parameter shifts due to temperature. Increasing interconnect life is accomplished by reducing the maximum current density guidelines, in traces as well as vias/contacts. A 5x reduction in maximum current density has proven reliable on a prior design. [4]

This work presents a linear voltage regulator and a frequency counter ASIC, integrating the final two required circuits for Quartzdyne pressure transducers. The voltage regulator is functional up to 250°C, while the frequency counter is functional to

275°C. Both ICs are designed and rated for powered life at 225°C.

Voltage Regulator ASIC

The original voltage regulator internal to Quartzdyne hybrids is a voltage reference with a discrete transistor regulator amplifier. The current voltage reference is now obsolete in die form. The expertise gained from the previously reported Oscillator ASIC design [4], enabled a regulator ASIC solution. A current-limited low-dropout 2.5V linear regulator replaces the original circuit. Adding a microprocessor reset saves three additional hybrid components. The solution will save 11 components in the overall hybrid circuit, and eliminates discrete transistors altogether.

The limited voltage reference supply forced the design to be based on simulations run with the foundry provided models. The circuit uses N-FETs, P-FETs, a BJT, and three types of resistors, 96 corners altogether. Tailoring the corners to the particular simulation reduces the total simulation time significantly. The design goals are summarized in Table 1, and Figure 1 shows the system schematic.

Voltage Reference

The band gap circuit is based on a common CMOS design shown in Figure 2. The circuit balances a proportional to absolute temperature (PTAT) current and complementary to absolute temperature (CTAT) voltage to generate a constant output voltage. Iptat is generated by D1, D2, R3 with I_{rat}=8; Vctat is generated by D1.

$$Iptat = \left(Vt \ln(Irat) + Voff\right) / R3$$

$$Vref = Iptat \times (R3 + R1) + VD1ctat$$

Resistors are implemented using a 130Ω/□ 350ppm/°C polysilicon resistor. Each resistor is based on one element, whose length and width is designed to minimize contact resistance effects and overall resistance variation. R2 and R3 are designed using series elements, while R3 is a combination on series and parallel elements. D1 & D2 are vertical PNP transistors whose layout rejects process and temperature variations from four sides. The transistor layout and current densities are chosen to maximize the linearity of I_{ptat} and VD_{ctat} throughout the temperature range.

The error amplifier is an Operational Transconductance Amplifier (OTA) with a P-FET output transistor. The OTA is biased with a temperature and process independent bias generator. Amplifier offset is kept to a minimum by using larger transistors and common centroid layout techniques. The offset voltage is simulated using Monte Carlo transistor parameter variation based on individual gate area. A 100 iteration Monte Carlo simulation shows the OTA offset voltage to be ±13mV max with a standard deviation of 3.9mV. This offset voltage significantly changes I_{ptat}, resulting in significant output voltage error. This presents the major limitation in a voltage reference design without trim options.

Table 1 Target Specification

Regulator	Min	Max	Notes
Vin	2.7V	5.5V	
Vout	2.45V	2.55V	
Icc		600µA	
Temp	-40°	225°C	
Iout		15mA	
Drop-Out		0.2V	15mA,225°C
Stability	0.1µF	5µF,15mA	
Load Reg.		1mV/mA	
Line Reg.		10mV/V	
Reset Level		90%Vin	
Delay	10uS		
Hyst	100mV		
OverCurrent	50mA	100mA	

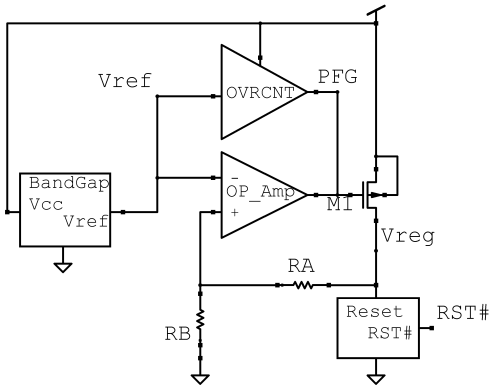

Figure 1 Voltage Regulator IC

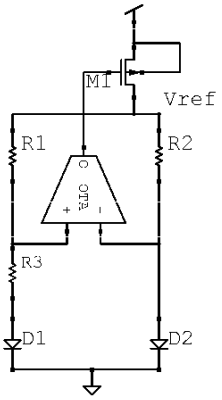

Figure 2 BandGap Voltage Generator

Voltage Regulator

The regulator design is a compensated two-stage op-amp with an additional output power

transistor, M1. The output transistor is implemented as a 200 finger device. Due to the low drop-out, extra care is taken with the design of the contacts, vias and metal widths. Stability is achieved with lead compensation using a poly silicon resistor and a poly1-2 capacitor. Since the low voltage design contains no cascoded amplifier stages long length transistors (8-12x L_{min}) reduced line regulation. Output voltage scaling is achieved with a 1200Ω/□ polysilicon resistor using the same layout techniques as the voltage reference.

Questions about foundry model accuracy at 225°C, process corner effects, no trim options, and the cost of failure led the design to be implemented as 5 IC's. RA's resistance (Figure 1) is varied to provide these output voltages 2.450V, 2.475V, 2.500V, 2.525V, 2.550V. This trades yield for confidence in obtaining Known Good Die (KGD).

The overall yield is simulated using Monte Carlo parameter variation based on individual device area. The resulting average, standard deviation and output scale factors can be used to estimate the overall yield to be approximately 14% for parts tested at both 30°C and 200°C.

Microprocessor Reset

The reset circuit consists of a reference based power on reset circuit shown in figure 3. The circuit is designed to reset at 2.2V on power up, with hysteresis on power down. The power on reset trigger point is set with a voltage divider; M1 provides the hysteresis. A low current transistor (M3) and a C1 provide the power up delay. Power down delay is minimized via a higher current transistor M2.

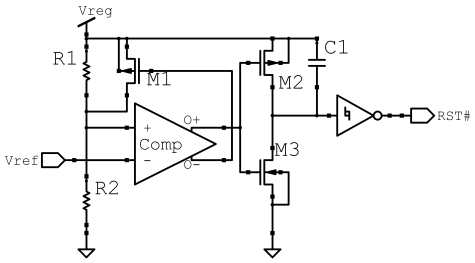

Figure 3 Microprocessor Reset

Current Limiting

Figure 4 outlines the basic operation of the current limiting circuit. The current source is generated by a scaled version of the output power transistor. When the voltage on R1 reaches V_{ref}, the output power transistors gate-source voltage is limited by M2. Because M2 is tied to V_{in}, its ability to reduce the output current is greatest at Vin=5.5V. The result is that the current limiting is sharper at V_{in}=5.5V than at 2.7V. The resulting limit current was higher than desired due to the softer limit at V_{in}=2.7V.

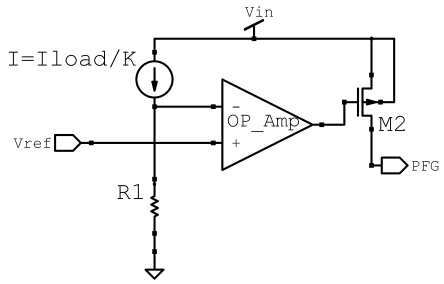

Figure 4 Current Limiter

Test Results

Initial characterization on 4 of each IC (20 total) between 25°C and 250°C was done on ICs assembled into hybrid modules. Temperature was controlled with a custom test fixture designed for hybrid circuits. The temperature accuracy is ±1.5°C at 25°C but increased to ±3°C at 250°C.

Figure 5 shows the output voltage vs. temperature on selected ICs. It is clear that many outputs take a significant upturn above 175°C, while some are flat to 225°C. The average output variation from 25°C to 200°C is ±0.54%, while the max is ±1.3%; from 25°C to 225°C the average is ±0.91%, while the max is ±1.75%. This data shows that sorted chips will be usable up to 225°C, with an increased yield loss. Current draw is 230µA at 25°C and increases to 340µA at 225°C.

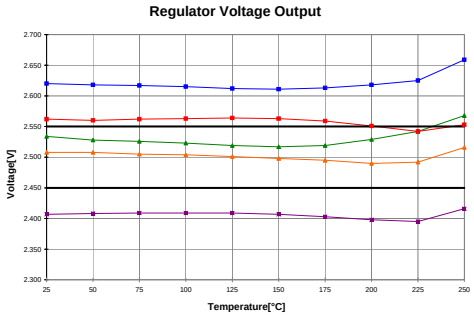

Figure 5 Voltage Regulator Output

A total of 9000hrs of 5.0V 225°C powered life testing on six IC's is ongoing. The IC's are configured with two load currents, 7.5mA and 15mA (I_{max}). Some outputs show 15-16mV of drift while a few ICs only drifted 5-8mV. No notable difference between the 7.5mA and the 15mA units drift is present. Results are plotted in Figure 6.

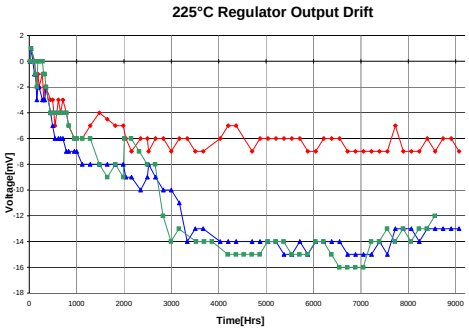

Figure 6 Regulator Drift

The measured dropout voltage at three temperatures with a load current of 16.5mA is shown in Figure 7. The average drop out at 225°C is 187mV, while the worst case is 198mV. The average dropout at 25°C is only 139mV. The test module increased the drop out by 2-5mV due to a series resistance inherent to the hybrid substrate metallization. A 15mA 225°C dropout equivalent can be calculated as 168mV average and 178mV max.

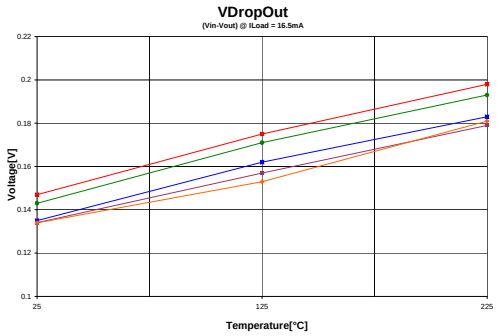

Figure 7 Dropout Voltage

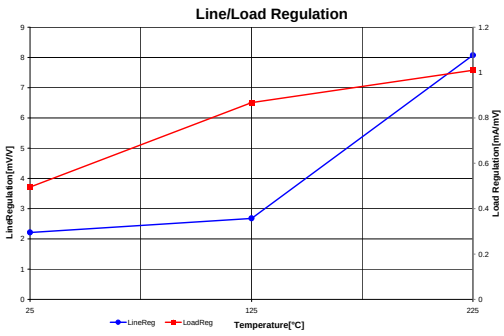

Figure 8 Line and Load Regulation

The output voltage was measured at V_{in}=4.1V and 5.5V, providing a line regulation estimate. The average line regulation vs. temperature is shown in Figure 8. Line regulation increased with temperature as a result of decreasing transistor output resistance. The worst case is almost 18mV/V at 225°C; the average is 8mV/V.

The output voltage measurements with a 5mA load and a 16.5mA load are used to estimate the load regulation. The load regulation is plotted in Figure 8, on the secondary axis. The worst case at 225°C is 1.3mA/mV, while the average is 1.0mA/mV.

Average reset threshold and hysteresis measurements are plotted in Figure 9. The max threshold is 91.5% while the min is 85.5%. The hysteresis decreases with temp due to M1's on resistance increasing with temperature. The chip to chip variation in hysteresis is about 70mV. Current limiter measurements show the expected soft and sharp limiting at 3.0V and 5.0V respectively. The limiting occurs around 75mA.

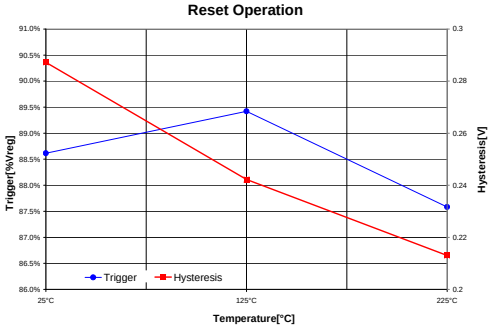

Figure 9 Reset Operation

Given that the output voltage tends to increase at higher temperatures a two point production IC screen is required. IC's are tested at both 30°C and T_{max} (200°C or 225°), parts that are within spec at both temps pass. The current production yield on wafers screened for T_{max}=200°C is 14.3%. The yield on a partial wafer sorted for T_{max}=225°C is 12.7%. Due to the large number of die on a wafer, the low yield still provides enough KGD for production use. The resulting regulator IC is shown in Figure 10.

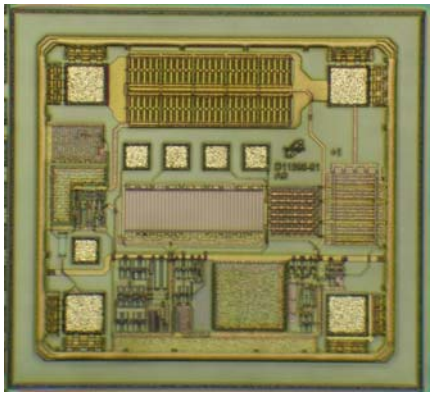

Figure 10 Regulator IC 48x43mil

Frequency Counter ASIC

The current Digital Quartzdyne Pressure Transducers contain an FPGA implemented as a frequency counter. Pressure and Temperature frequencies are counted using a 7.2MHz Reference signal and the results are communicated via an I^2C compatible bus. In contrast, a Quartzdyne Analog transducer does not count the pressure and temperature frequencies.

The FPGA is a high cost, low yield part that draws excessive current at 225°C. Expertise gained from the previously reported Oscillator ASIC [4] suggested a digital ASIC as an option to replace the FPGA. Transistors and logic gates from previous test chips showed functionality up to 300°C, increasing the chances of success. Converting the FPGA to an ASIC had the potential to reduce cost, reduce power consumption at high temperatures, have fewer gates, reduce die size, and reduce the number of parts in the system.

In addition, some new features were proposed for the customers benefit: a reference output, configurable pressure and temperature output and a data checksum. To ensure a smooth integration into existing customer designs backwards compatibility was required.

Design Approach

Proven FPGA code served as an initial design specification and reduced the design effort. A custom IO ring was designed to interface directly to the oscillator IC and the customer's electronics eliminating six hybrid components. The addition of a JTAG scan path increased testability. The addition of unused gates allowed for small design changes and bug fixes using a process hold at the foundry. Selective handcrafted layout reduced die size and increased performance.

Simulating with a higher clock speed mimics the high temperature, 2.5V V_{cc}, and slow process corner effects on the logic gates. The Foundry-provided 3.3V ambient temp models were used with an increased clock speed for simulations. A high temperature probe card was used for in house debugging and production test development.

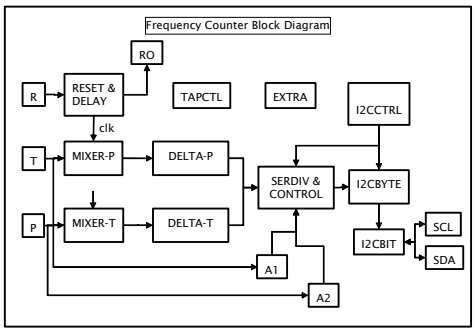

Figure 11 Digital ASIC Block Diagram

Frequency Counter Operation

The block diagram in Figure 11 details the operation of the chip. Three crystal frequencies are transmitted to the Frequency Counter ASIC from the oscillator chip. The 7.2MHz reference signal serves as the clock. The DELAY block waits on startup for 8mS to allow the oscillators to settle. The MIXER blocks synchronize the inputs so they may be counted.

All three frequencies are continuously counted in the DELTA blocks. Upon a data request the counts are loaded into the serial divider block, SERDIV, and then the 4 byte integer result is written to the I^2C bus. The time between data requests is called the gate time and ranges from 1.0mS to 2.3S.

The effective limit of resolution is determined by the number of counts of the reference frequency NR = TG * FR (approximately 1 part per 7.2 million per second). Increased gate time will give better resolution. XP and XT are used with calibration coefficients to calculate pressure and temperature. XP and XT are related to the counts (NP, NT, NR) and frequency (FP, FT, FR) as follows: [5]

$$XP[nbits] = NP \times \frac{2^n}{NR} = FP \times \frac{2^n}{FR}$$

$$XT[nbits] = NT \times \frac{2^n}{NR} = FT \times \frac{2^n}{FR}$$

The I2CCTRL controls the SERDIV and CONTROL blocks which contain the ChipID as well as Control and Status bits. The TAPCTL block controls JTAG scan operations and the EXTRA block represents various extra gates scattered throughout the chip.

Design

Several custom IO cells were designed: a Schmitt trigger to interface to the oscillators, a bidirectional open drain transceiver for the I^2C

compatible bus, and a high drive output buffer to directly drive the application load. Level shifters allow for a low voltage core (2.5V) and a higher voltage IO for external communications (2.5V-5.5V).

A clock speed derating factor was found by simulating logic gate speed; the results are shown in Table 2.

Table 2 Simulation Derating Factors

Description	Derate Scale
25°C to 225°C	1.5x
3.3V to 2.5V	1.5x
Worst Case Slow Corner	1.9x
Overall	4.3x -> 4.6x

The foundry-provided models are valid at 3.3V and ambient temperature. Simulation with a 33MHz reference signal provided some margin for error. The existing FPGA code was modified with the new features and working test waveforms were used to maintain backwards compatibility.

The checksum feature provides a level of data integrity. Data is read in four byte chunks followed by a 5th byte checksum. The check sum is calculated by adding all 5 bytes together. A valid checksum results in zero when the carry bits are dropped. The five byte data stream is repeated until the host acknowledges the transmission.

A reference out pin was added to serve as a clock for digital systems. The power up default configuration is 7.2MHz and can be changed to 1KHz through the I^{2}C bus. The address of the device is latched on power up, after which the address pins can be configured as pressure and temperature outputs via the I^{2}C bus.

The addition of a JTAG scan path was added for pre-loading counters and testing boundary conditions not practical otherwise. This feature saves production screening time and cost.

Layout

A first pass core layout was implemented as a standard cell place & route design shown in Figure 12A. It is 211 x 151 mils, the resulting chip using this layout would have been close to the size of the current FPGA. By partitioning the design at the module level a 2.3x size reduction was achieved, Figure 12B. Hand packing two of the large math modules into regular structures resulted in an additional 3.1x over the partitioned version for a total of 7.2x size reduction. The result was a 50mil x 89mil core shown in Figure 12C.

The top level routing was done by hand with special attention given to clock routing, power routing, and critical signal routing. A custom delay calculator combined with extracted capacitance was used to simulate realistic timing delays. Signal

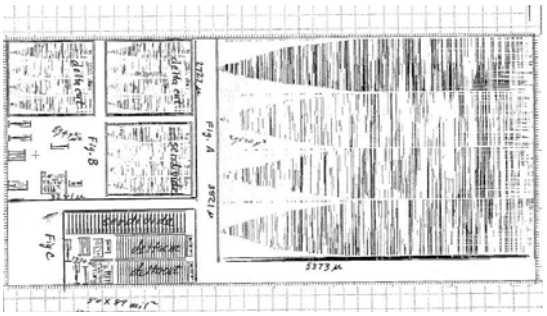

Figure 12 SPR Comparison

buffers were adjusted as necessary, and the process was repeated until timing was met. Extra-gates were interspersed in the layout for ease of use. The IO ring was hand placed and routed to the core. Figure 13 shows the final die layout.

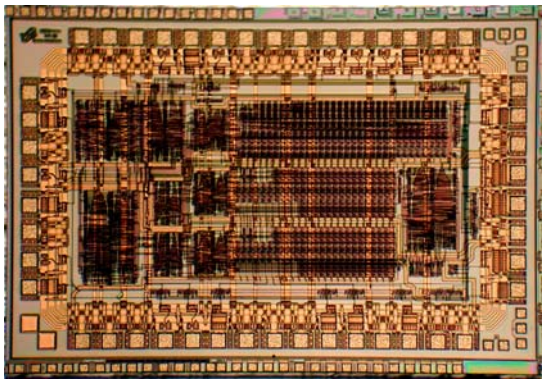

Figure 13 Digital ASIC Die Photo

Fabrication

The final layout was sent to the foundry for fabrication. Six wafers were ordered with a hold of three wafers after METAL-1. Two of the first three wafers were returned and preliminary tests were done in-house. These tests showed functionality above 250°C with lower current than the FPGA based hybrid. Some minor bugs were also found. After fixing the bugs using extra gates and modified METAL-2 and METAL-3 masks the final 3 wafers were finished and fabricated. The second pass die were fully functional

Testing

The TRI-ASIC prototype hybrids are functional up to 275°C exceeding the goal of 225°C. Current vs. temperature measurements, shown in Figure 14, are relatively flat up to 225°C. The new ASIC based design starts increasing supply current at 225°C while the FPGA starts the increase 50°C lower at 175°C.

A production screening vector set was developed in house using a high temperature probe card. This step was useful in providing good vectors

to the test vendor. Some timing issues were found relating to asynchronous paths when dynamically changing pin options and activating test structures on the chip. These issues do not affect the normal operation of the system. Current production screening yields 91%.

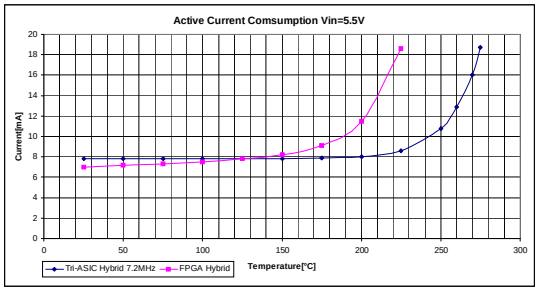

Figure 14 FPGA vs ASIC Module Current

Qualification

Qualification was completed on prototype hybrid modules. Four transducers surpassed 1000 hours of powered life at 225°C and three hybrid circuits surpassed 1000 hours of life cycle to 250°C, including 100 metal to metal shocks. Design qualification was finalized with successful calibrations.

Hybrid Circuit Comparison

Hybrid circuits based on both the regulator and the digital ASIC have been manufactured. The resulting circuits consume less current, are easier to manufacture and more reliable. Figure 15 shows the resulting hybrids compared to pre-ASIC equivalents. It is clear that each ASIC made its mark on the hybrid. The regulator ASIC saves 11 components, and eliminates the last remaining discrete transistor. The digital ASIC saves direct cost in parts eliminating six components and freeing up space for added ESD protection.

Conclusion

A High Temperature linear voltage regulator and a frequency counter have been designed using a 0.8µm bulk CMOS process. The voltage regulator is functional to 250°C and rated for long term operation at 225°C. It features a 2% tolerance 2.5V output, with a 0.2V dropout. Powered life data showed 0.6% downward drift at 225°C. Chips are tested at 30° and 200°C(or 225°C) for production sorting. Overall yield is consistent with estimates, providing enough parts for production. Transducers using this chip starting shipping in January 2009. The project

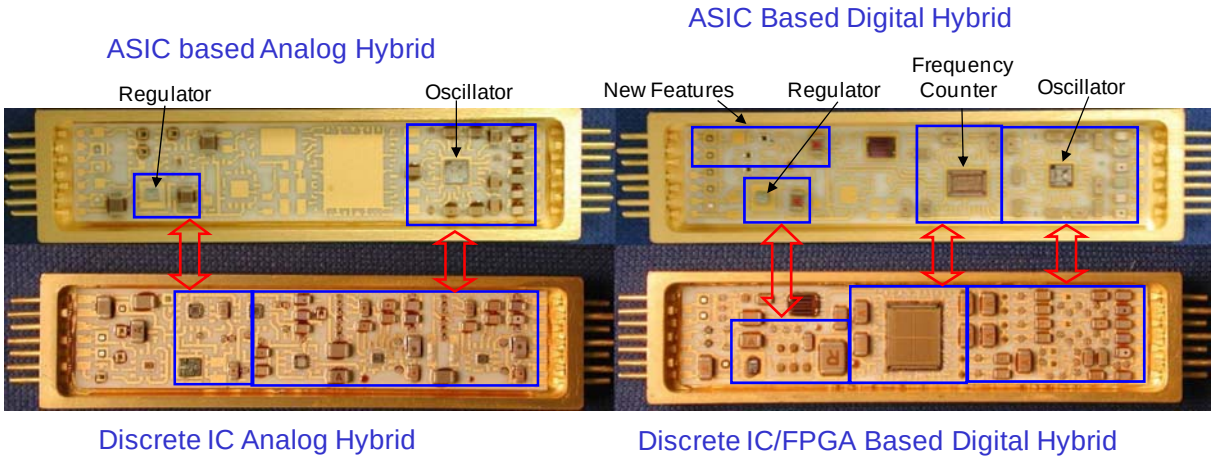

Figure 15 Hybrid Circuit Comparisons

successfully replaced an obsolete voltage reference, a few other parts, and eliminated discrete transducers from the hybrid circuit.

The FPGA based frequency counter has been successfully converted to a 225°C rated digital ASIC. New features including a reference signal output and a checksum byte on all four byte data reads. Custom block layout reduced the resulting chip 3x over its predecessor. The custom IO ring replaced 6 hybrid components. Tests show that modules built using this IC are functional to 275°C, while consuming 2.3x less current at 225°C. This combined effort completes the integration of the three required circuits for high precision quartz based transducers. Transducers based on these two new chips and the oscillator IC began production in August 2009.

References

[1] Shoucair, F.S. “Design Considerations in High Temperature Analog CMOS Integrated Circuits.”, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Sept. 1986, pp. 242-251

[2] Richard Brown & Koucheng, Wu. “Scaling CMOS Design Rules for High-temperature Latchup Immunity.

[3] Pect, Micheal. “The Influence of Temperature on Integrated Circuit Failure Mechanisms.”, Quality and Reliability Engineering International, May-June 1992, Vol. 8, No 3, pp.167-175.

[4] Rose, Shane. “A 225°C Rated ASIC for Quartz based Downhole Transducers” HITEN 2007, (www.quartzdyne.com)

[5] Quartzdyne Inc., “Digital Pressure Transducer Operating Manual” , s.n. 2009

[6] Quartzdyne Inc. “Operating Manual for Quartzdyne Digital Pressure Transducer”, s.n, 2009

[7] Richard S. Muller, Theodore I. Kamins “Device Electronics for Integrated Circuits”, John Wiley & Sons, 1986

[8] David Johns, & Ken Martin “Analog Integrated Circuit Design”, John Wiley & Sons, 1997

[10] Gabriel Ricón-Mora, “Voltage References, From Diodes to Precision high-order Bandgap Circuits”, John Wiley & Sons, 2002