

# A 225°C Rated ASIC for Quartz Based Downhole Transducers

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## Abstract:

*Quartzdyne Pressure Transducers incorporate circuits that require operation at high temperature, low voltage, and low power. The next-generation circuit design includes additional features that require more components; to fit in the same space, a higher level of circuit integration was required. Die component selection is typically limited to a few simple devices; these same parts are becoming unavailable, further limiting the selection. Experience has shown that reduced component count decreases circuit failures due to high vibrations and mechanical shock while increasing its life. Using a custom high-temperature ASIC to replace many of the discrete components of these designs would be desirable, if the development costs were reasonable.*

*High temperature rated SOI and standard bulk CMOS processes were investigated. The SOI did not meet the design criteria as it would not allow analog circuit design at 2.5V. Bulk CMOS was shown to enable low voltage analog design for high temperature applications. The mask costs associated with a 0.8 $\mu$ m feature size have become relatively inexpensive; combining this with the availability of small engineering wafer runs provides lower cost small volume ASIC manufacturing. Using a 0.8 $\mu$ m Bulk CMOS process, low-cost CAD tools and well-known high temperature CMOS design techniques, a 225°C rated ASIC was developed, fabricated and tested.*

*This ASIC (88mil x 92mil) powers the three-crystals of a Quartzdyne Pressure Transducer, providing 3 amplifiers with startup control, 2 mixers with filters, independent bias generators as well as output level translators. For crystal design flexibility, each oscillator's gain is adjustable through 2 external tank capacitors and one bias resistor. The startup control requires one external capacitor for each oscillator. Full circuit functionality was demonstrated -40°C to 275°C. A new hybrid circuit was developed utilizing this ASIC, it has reduced the overall component counts 40% to 55%. Because the manufacturing costs have decreased through higher yields and increased throughput, the ASIC development costs have become reasonable.*

## 1. Introduction

Quartzdyne pressure transducers provide precision measurement in various down-hole and subsea applications where temperatures range from -40°C to 225°C and supply voltage ranges from 2.7V to 12V. The transducer is based on 3 quartz crystals, one pressure sensing, one temperature sensing, and a stable reference. The oscillator circuit powers the 3 resonators converting their natural resonant frequencies into easily countable signals. The reference signal provides a stable clock for counting.

The design of the required circuitry has been challenged by a limited selection of high temperature operational die components. Discrete transistors and simple ICs tend to be the only dice that operate at elevated temperatures, these parts are becoming obsolete. New oscillator features require more components without increasing the circuit size, requiring a level of integration that is unrealistic using the available component selection. Experience shows that reduced component counts increases overall circuit reliability while decreasing manufacturing costs.

New circuit features, a continuous desire to increase reliability, and a reduction of dependency on parts that are becoming obsolete have provided an immediate need for an ASIC. To provide the necessary transducer performance this chip needs to operate over a wide temperature range(-40°C to 225°C), at 2.5V, provide low sensor output signal jitter(<200nS), low crystal drive level(10uW), Startup Control, 50% Duty Cycle Outputs, and long term reliability (5+years at 200°C).

## 2. Process Choice

The two process technology options considered are bulk CMOS with a commercial temperature rating and high temperature rated SOI CMOS. Bulk CMOS has well documented issues with leakage currents and latchup at elevated temperatures, however many custom IC designs as well as commercially available parts have been shown to work at or above 200°C.[1][2] Some examples of commercial bulk silicon parts that function at high temperatures are the REF191 (200°C), LT1019 (240°C), 74VHC14 (275°C) and LM3046 (250°C+). Bulk silicon is a viable option for 225°C ASICs.[3,4,12] Custom ICs designed using High Temperature rated SOI processes have been shown to function above 300°C.[5] These processes have very high threshold voltages which severely limits the ability to design 2.5V amplifier circuits.

Several reliability issues must be considered when designing high temperature ICs. Among them are electron migration, gate dielectric breakdown and hot carrier effects. Electron migration can be dealt by redefining the current density limits. Solutions to gate dielectric breakdown are limited to process selection and supply voltage reduction. Hot Carriers are a reliability problem for all CMOS, high temperature does not increase its effect but longer length analog devices can reduce the effect.[3]

Many semiconductor foundries only support the sophisticated expensive CAD tools. Smaller designs don't need the advanced CAD software; lower cost tools are currently available for \$25K. Silicon foundries that support these tools greatly reduce the initial costs of designing simple ICs.

XFAB Bulk CMOS processes satisfy the low voltage requirement, as well as low cost CAD support. Low volume engineering runs are available as well as multi-project runs (MPW) and multilayer mask (MLM) runs. There are 3 reasonable processes to choose from: 0.6 $\mu$ m, 0.8 $\mu$ m, and 1.0 $\mu$ m. The 0.6 $\mu$ m process was eliminated since it had the thinnest gate oxide which provides the least resistance to gate dielectric breakdown. The 1.0 $\mu$ m process was eliminated due to a lack of support for MPW runs and lower transistor gain. For these reasons the 0.8 $\mu$ m process was chosen for this and future projects. Total manufacturing costs associated with the 0.8 $\mu$ m process are very reasonable for engineering runs, with MPW runs being far less.

### 3. Layout Design Techniques

Successful layout techniques designed to prevent latch up have been shown.[6] These techniques are similar to IO design guidelines. The goal is to reduce the gain, and the transient Vbe of the parasitic BJTs. Gain reduction can be accomplished by increasing the separation of the n-FET drains to the n-well edge as well as the p-FET drains to the p-substrate.[4,6,10] The transient base emitter voltage can be reduced by decreasing the substrate/well contact to source resistance. Using butting substrate contacts along the width of the transistor reduces the source to body resistance significantly.

Electron migration effects can be reduced by adjusting the max current density of the metal traces. Using a conservative assumption that the foundry derives its metal current density limits based on 125°C and 10 years life and 0.7eV activation energy on Al-Cu-Si, a new guideline can be defined for 225°C and 4 years.[3,7] The result is the foundry's current density guidelines were scaled down by 5x for all metal layers as well as vias and contacts. To further eliminate the potential for hot carrier reliability problems, no transistors were designed at the minimum length. The majority of transistors were designed with 1.6 $\mu$ m lengths, with only a few at 1.2 $\mu$ m. Drain leakages can easily be reduced 2x by simply splitting FETs in two (interdigitizing) then sharing drains as well as using minimum drain area devices. All these techniques were used in this design to increase the max operating temperature and the long term reliability of this chip.

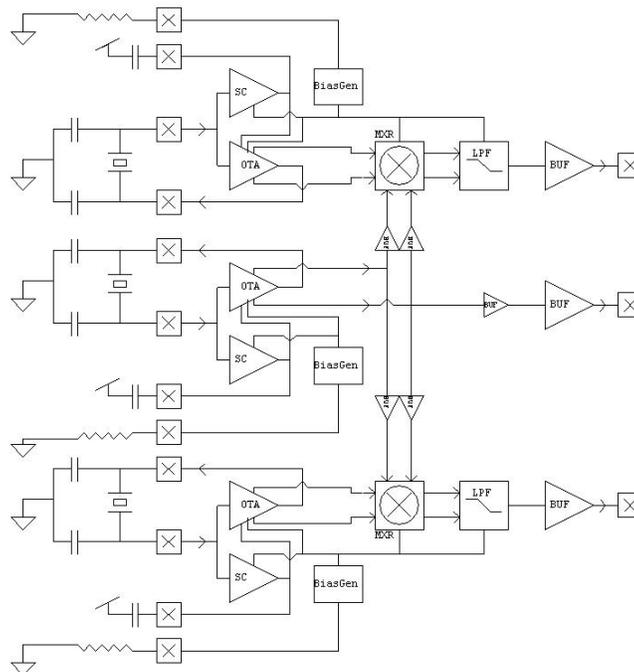


Figure 1 System Schematic



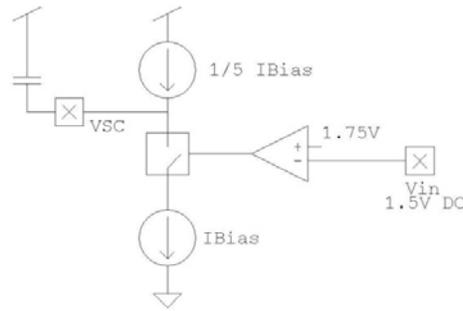


Figure 3 Start Up Control Schematic

## 7. Start Up Control

The start up circuit consists of a peak detector and an open drain sink output with internal current source pull up. The peak detector is a comparator whose positive input is biased 0.25V above the DC bias of the oscillator and the negative input is tied to the oscillator input. The output current sink duty cycle is controlled by the oscillator peak-to-peak voltage ( $V_{pp}$ ). The minimum oscillator  $V_{pp}$  is determined by the ratio of source to sink current and the DC difference in comparator input voltages. Oscillator  $V_{pp}$  above the minimum will decrease VSC (figure 3), voltages less than the minimum will increase VSC. To ensure operation over a wide temperature range, the current sink and source are based upon the same constant gm bias generator. Only one external capacitor is required for filtering.

## 8. Mixer

Mixing is accomplished with a differential input and output Gilbert cell. A layer of isolation between the reference signal inputs and the sensor inputs was implemented to reduce the potential of cross talk. The output signal is filtered with two capacitors and converted to single-ended utilizing a hysteretic comparator.

## 9. Output Buffers

This chip is intended to be the heart of both analog and digital output transducers. The digital version signal outputs need only to drive 2.5V rail to rail, where as the analog needs to drive 2.7V to 5.5V. IO power supply voltage bond pads are provided along with level translation to provide 2.5V to 5.5V outputs. The Buffer is a rail-to-rail output designed to drive a typical IC load (25pF@15nS).

## 10. Test Results

The circuit performance characterization of the initial 42 hybrid modules (12 analog, 30 digital) that have been built was completed with good results. Our standard test systems measure the signal jitter for both edges of the P and T output at 80ns to 150ns, within the design goal. Start up times are typically 130mS at  $T=amb$ , and worst case 200mS at 200°C. The output signal duty cycle is 48% to 52% on all three channels. The supply current has been verified to be 2.0mA at 25°C with 2.5V outputs. Several modules were shown to function up to 245°C, with the limiting IC being a LT1019 voltage reference. A test module was built using a high temperature Cissoid voltage reference was shown to function up to 275°C, with its limit being the oven and cable.

All Quartzdyne transducers are calibrated and receive their own unique calibration coefficients. A mixed model set of 12 transducers, with ASIC based hybrid modules, were calibrated a total of 19 times at various temperature ranges. The results are typical of transducer recalibrations with the original circuits, showing the new hybrid has no effect on calibration performance. Table 1 summarizes these results.

Table 1 Transducer Calibration Results

Temperature Range	Transducer Quantity	Number Calibrations	Average Error(%F.S.)
-40°C to 85°C	2	2	0.0081
25°C to 175°C	5	10	0.0125
25°C to 200°C	2	4	0.0093
25°C to 225°C	3	3	0.0185

Powered life testing on 6 ASIC based modules is ongoing. There are two separate tests, 3 analog modules at 225°C (figure 4B) and 3 digital modules at 200°C (figure 4A). Both tests have successfully surpassed 1000 hours of testing, the goal for the 225°C test is to reach more than 7000 hours showing a 5 year life at 200°C (2x/10°C derating).

### 11. Manufacturing Improvements

A new hybrid substrate using this chip has been designed. The new module allowed a significant component count reduction. (Table 2) The component count reduction allowed the hybrid substrate design to be configurable as either a digital or analog module. Figures 4A & 4B show the digital and analog component placements on the substrate. The new analog module placement looks to be missing a few components, that is not the case. The apparent lack of components is due to the level of integration internal to the ASIC. The other components in the analog module are for the regulator, the output cable buffer and ESD protection.

Table 2 Component Count Reduction Summary

New Module	IC's	Discrete Devices	Capacitors	Resistors
Digital (% inc/dec)	6(100%)	6(-70%)	25(-20%)	14(-60%)
Analog (% inc/dec)	4(-33%)	4(0%)	20(-33%)	9(-75%)

Figure 4 shows a good comparison between the two hybrid circuits before and after the ASIC was designed in. The left side is the digital modules, the right is the analog. The top two modules are the new version while the bottom is the prior version. It is especially clear in the new analog module how much circuitry was replaced with one IC. Looking closely at the digital versions a much lower component density was possible, this contributed to increasing the yields on hybrid modules.

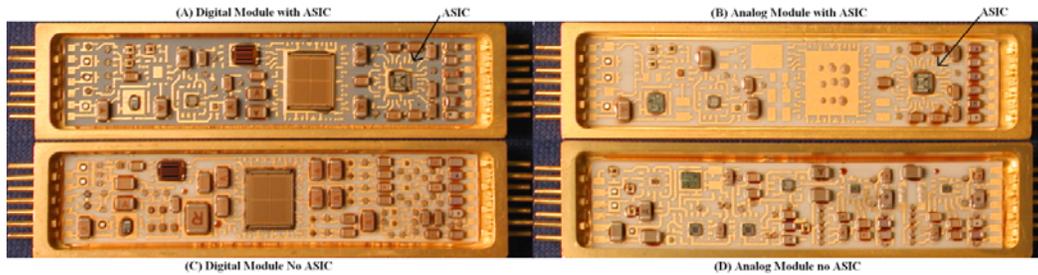


Figure 4 Hybrid Module Comparison

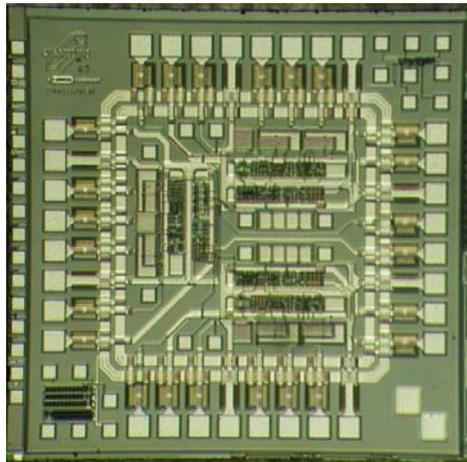


Figure 5 Oscillator ASIC Die

### 12. Conclusion

A custom Bulk CMOS ASIC to power quartz-based transducers has been developed. (figure 5) Total supply current is 2mA@T=amb while signal jitter is kept to <200nS. A new hybrid circuit has been developed utilizing this ASIC. The new design's viability has been shown through functionality test up to 275°C, standard Quartzdyne calibrations over a -40°C to 225°C range, and >1000hrs in powered life testing at 225°C. The component count reduction and new

hybrid substrate design guidelines have significantly increased the manufacturability of the hybrid. Increased hybrid module yields, decreased manufacturing times, and a reduced dependency on hard to find parts has provided ample justification for this IC.

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